

System Basis Chip CY329



FEATURES

- ▶ Automotive system supply, ASIL C (D) ready
- ▶ Suited for Permanent Supplied Systems (PSS) or Non-Permanent Supplied Systems (NPSS) with or without CAN wake-up
- ▶ VPR boost/buck regulator works down to 3V battery voltage
- ▶ Two 5V Linear voltage regulators
- ▶ Three independent 5V Sensor supplies
- ▶ Power stages (7x Low Side, 1x High Side) with integrated clamping and diagnosis
- ▶ CAN-FD transceiver
- ▶ MSC Micro-second bus μ C interface
- ▶ 4x 32 bit stop counter
- ▶ Level 3 watchdog
- ▶ TQFP64ePad

APPLICATIONS

- ▶ Engine Control Units

DESCRIPTION

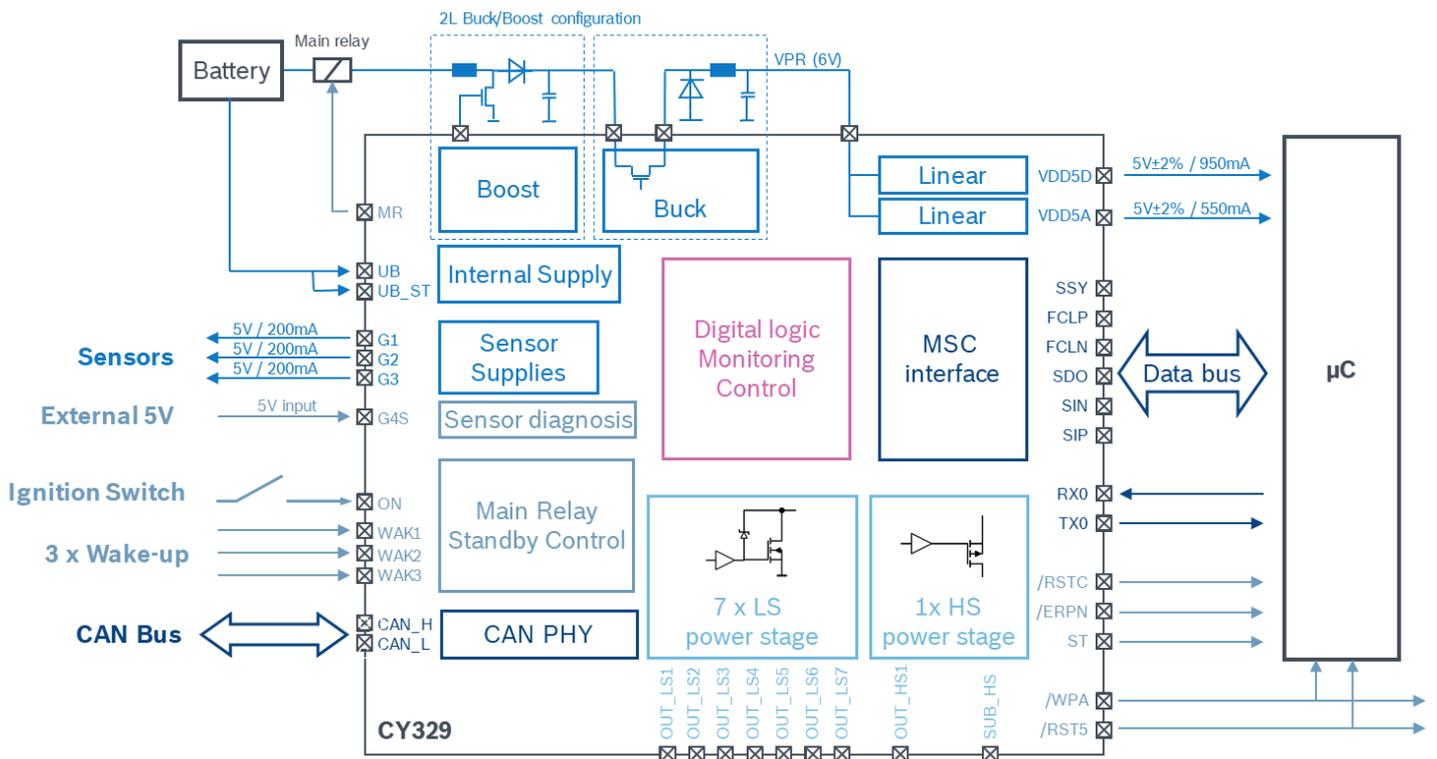
CY329 is a high-end system basis IC designed for Automotive Engine Control Units. It comprises safety features and a CAN-FD interface. With its supplies for ECU components, the chip can be applied to a wide range of ECUs. The high integration level benefits a small pcb footprint.

The integrated voltage pre-regulator (VPR) is implemented as boost/buck regulator with external switching MOSFETs, allowing for easier pcb design and less potential hotspot issues. The regulator provides a lot of flexibility in its application. It can be operated in single-coil as well as dual-coil configuration and offers a configuration pin for operation with different external coils.

The CY329 provides wide configuration options via the MSC interface, such as a direct control of [OUT_LS1...3] via [WAK1...3] pins or the shut-down delay of the power stages.

The MSC interface also gives access to a wide range of the status information, including the actual gate voltage of all power stages.

BLOCK DIAGRAM



System Basis Chip CY329

MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply voltage [UB] (static)	-0.3	40	V
Supply voltage [UB_STBY] (static)	-16	40	V
Voltage resistance, MSC pins	-0.3	6.3	V
Static wake-up pin [WAK1..3] voltage	-0.3	40	V
Static ignition event pin [ON] voltage	-0.3	40	V
CAN supply	-0.3	5.5	V
CAN_H, CAN_L (static)	-27	40	V
Static error pin [ERP_N] voltage	-0.3	6	V
Static error pin [RSTC] voltage	-0.3	6	V
Input current, static, EIN, WAK	-15	15	mA
Operating junction temperature (at T = 105°C, P_diss.= 2.8W)	-40	150	°C
ESD (IEC61000-4-2), CAN_H, CAN_L	-6	6	kV
ESD (HBM), CAN_H, CAN_L	-500	500	V
ESD (HBM), VDD5C, GNDC	-2	2	kV
ESD (CDM)	-500	500	V
ESD (CDM), corner pins	-750	705	V

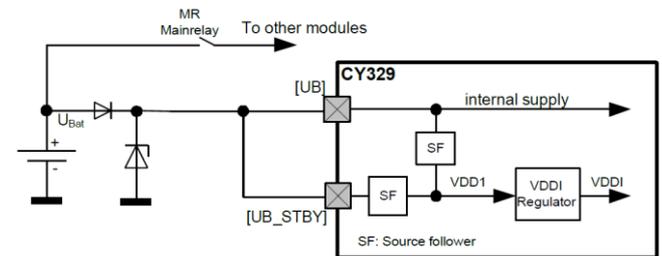
POWER SUPPLY

The CY329 can be supplied in 3 different configurations:

- Permanent Supplied Systems (PSS)
- Non-Permanent Supplied Systems (NPSS)
- Non-Permanent Supplied Systems with CAN Timer Wake-up (NPSS-CTW)

Permanent Supplied Systems (PSS)

In Permanent Supplied Systems (PSS) the ASIC pins [UB] and [UB_STBY] are connected directly to the battery supply U_{Bat}:

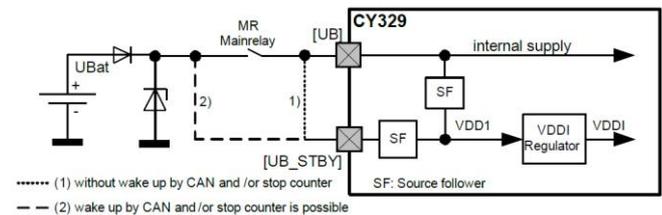


Non-Permanent Supplied Systems (NPSS)

In Non-Permanent Supplied Systems (NPSS) the ASIC pins [UB] and [UB_STBY] are connected via main relay to the battery supply U_{Bat} (see fig. below, note 1).

Non Permanent Supplied system with CAN Timer Wake-up (NPSS-CTW)

In Non Permanent Supplied system with CAN Timer Wake-up (NPSS-CTW) the ASIC pin [UB] is connected via main relay to battery supply. The ASIC pin [UB_STBY] is connected directly to the battery supply U_{Bat} (see fig. below, note 2).



Wakeup functionality

Switching on of CY329 is possible by T.15 pin [ON], by one of the wakeup pins [WAKx], wake-up via CAN or by a stop counter wakeup.

System Basis Chip CY329

VPR BUCK/BOOST CONVERTER

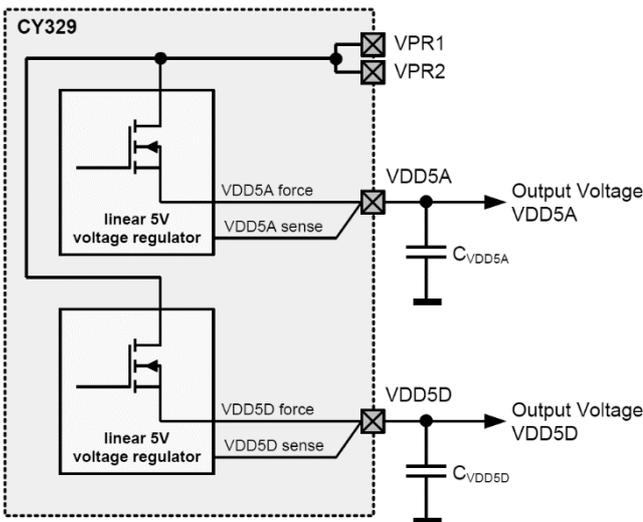
The Buck/Boost-Converter VPR is capable to provide a maximum output power of 18W.

To reduce the emission of the VPR Buck/Boost regulator a spread spectrum can be activated.

Parameter	Min	Typ	Max	Unit
V_{OUT_VPR} , $3V < V_{UB} < 40V$, Buck/Boost mode	-3%	6.0	+3%	V
Max. load current, $V_{UB} > 4.5V$			2.8	A
Max. load current, $V_{UB} > 3.2V$			2.0	A
Switching frequency	480	500	520	kHz

VDD5 LINEAR SUPPLY

The VDD5 linear supplies consist of VDD5A and VDD5D regulator. The VDD5 regulators are realized as a linear regulator with an internal n-channel MOSFET power stage. VDD5A is suitable for analog supply and as reference voltage for the sensor supplies. VDD5D is a 5V power supply e.g. for supplying uC and CAN.



Each output VDD5A and VDD5D is monitored for **undervoltage**. In case the voltage at one of these pins drops below the undervoltage threshold V_{VDD5_UV} the RST5 pin is pulled to LOW. When the voltages at both VDD5A and VDD5D exceeds V_{VDD5_UV} again, the pulldown at RST5 pin is not immediately released, but extended by a reset filter time.

Each output VDD5A and VDD5D is monitored for **overvoltage**, indicated by MSC-bits. The indication can be routed to the [WDA] pin.

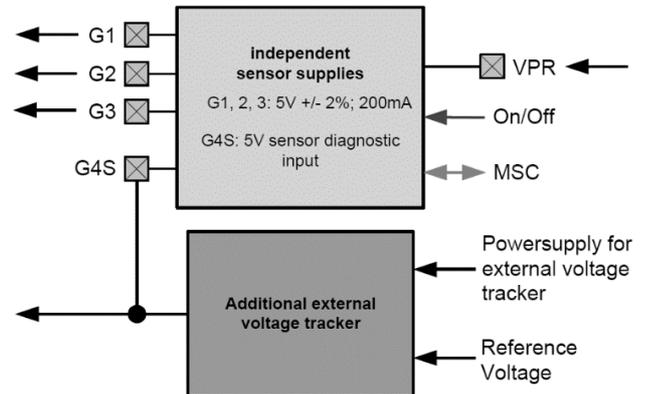
Furthermore, an **overtemperature monitoring** is implemented. The status can be read via a MSC bit. When T_j exceeds the overtemperature threshold nearby the output stages VDD5A and VDD5D, the bit is set.

VDD5A and VDD5D ramp-up simultaneously. During ramp-up, the mismatch between VDD5A und VDD5D depends on the external circuitry.

Parameter	Min	Typ	Max	Unit
V_{OUT_VDD5A}	4.9	5.0	5.1	V
I_{VDD5A}			550	mA
V_{OUT_VDD5D}	4.9	5.0	5.1	V
I_{VDD5D}			950	mA
Mismatch between VDD5A and VDD5D			0.75	%
VDD5 softstart time		2.0		ms

5V SENSOR SUPPLIES

The CY329 contains 3 independent sensor supplies G1, G2, G3 and one 5V diagnosis input G4S.



The sensor supplies G1, G2, G3 can be switched off and on individually via writing to a MSC register. Default setting after reset is, that all sensor supplies G1, G2, G3 are on.

At start-up, all sensor supplies are switched on simultaneously together with the VDD5A regulator. The ramp up synchronization to VDD5A depends on the load capacitance at the pins [G1], [G2], [G3]. VDD5A is the reference voltage for G1, G2, G3.

The sensor supply unit comprises also a monitor for an external 5V supply, referred to as G4S. The reference for the voltage monitoring is VDD5A.

Each sensor supply G1, G2 and G3 and the monitoring input G4S offer the following monitoring and protection capabilities:

- Protection against **short-circuit** to battery (SCB) and ground (SCG). In case of SCB, a reverse current flow to [VPR] will be avoided by a back to back output stage.
- monitoring for **under-** and **overvoltage**.

System Basis Chip CY329

- monitoring for **overcurrent** (only G1, G2, G3). In case of such an event, the supply pin is deactivated after a configurable debounce time.

The sensor supply output stage is equipped with an **overtemperature monitoring**, resulting in a thermal shut down in case of exceeded temperature. The shut down is implemented in such a way, that the output voltage is reduced with increasing temperature, starting about 5°C below the thermal shut off temperature.

Parameter	Min	Typ	Max	Unit
V_{OUT_Gx}	4.9	5.0	5.1	V
Total current capability G1+G2+G3			200	mA
Temperature for thermal shut off Gx ramp-up time		165 4.5		°C ms

MICRO SECOND CHANNEL (MSC) INTERFACE

The MCU can communicate with the CY329 via the bidirectional MSC interface.

The MSC is a serial interface, which is especially optimized to connect peripheral devices via serial link to a microcontroller. The serial communication link is built up by a fast synchronous downstream channel from the microcontroller to the ASIC and an asynchronous upstream channel (referenced to downstream clock). In the downstream interface, the FLC (clock) and SI (data) inputs use low voltage differential signaling (LVDS), the SSY (select/sync) input and SDO (data) output are single ended.

Multiple devices with MSC on a single downstream connection are possible. Selection of a device for downstream communication is done by separate [SSY] signals while the FCL, SI and [SDO] signal lines are shared.

MONITORING MODULE (WDG)

The monitoring module generates questions to the MCU in a defined sequence, which has to be answered by the MCU within a certain (configurable) time frame. The question has a length of 4 bits, while the expected response has a length of 32 bits.

A sophisticated logic allows for escalation schemes in case of missing, non-correct or badly timed MCU responses, helping to discriminate between simple and more severe error conditions.

Beside the MSC interface, the monitoring module has two open-drain output pins [WDA] and [ERPN] in order to indicate states to the MCU.

RESET CONTROL

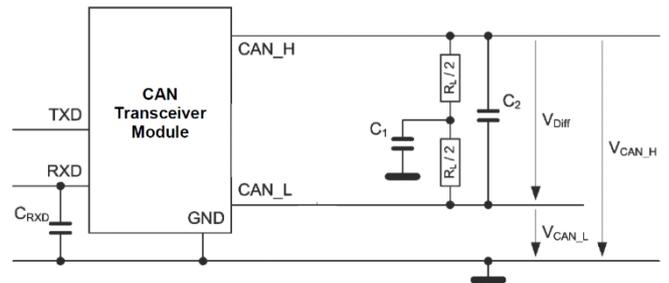
The CY329 offers two pins to indicate a reset condition, [RST5] and [RSTC]. They are triggered if

- certain undervoltage conditions occur
- or by a MSC command
- or by the monitoring module (watchdog).

The [RST5] and [RSTC] pins are bi-directional, so that external trigger signals can be detected and evaluated by the ASIC as well.

CAN TRANSCEIVER

CY329 implements a CAN-FD interface with a maximum bit rate of 5 Mbit/s. The interface offers different operating modes (Normal, RxOnly, Standby, Sleep, HighZ) and various configurable wake-up mechanisms.



Parameter	Min	Typ	Max	Unit
[TX0] input LOW level			0.9	V
[TX0] input HIGH level	2.1			V
[RX0] input LOW level			0.4	V
[RX0] input HIGH level	$V_{VDD5D} - 0.4$		V_{VDD5D}	V
External load at [RX0]			25	pF

STOP COUNTER

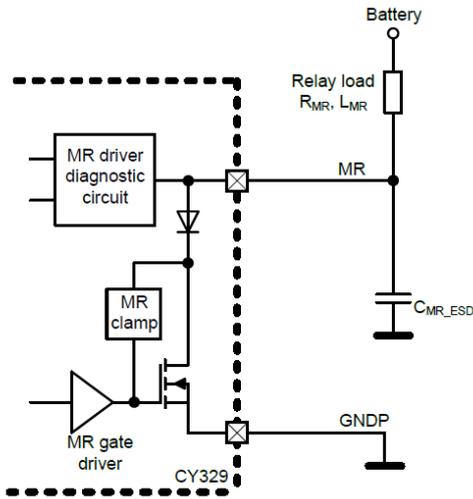
The CY329 comprises a stop counter module, consisting of four individual 32 bit counters with a resolution of 1s or 100ms. The counters can be used for simple counting, time measurement, and can trigger a wake-up or a delayed system shutdown.

MAIN RELAY DRIVER

The main relay driver is a reverse-polarity protected low side driver stage at the [MR] pin with integrated clamping and short-circuit protection.

System Basis Chip CY329

The main relay driver is switched on and off as part of the ramp-up and ramp-down sequences, respectively.



With the diagnosis circuit of the main relay stage the following error states can be detected:

- short circuit to battery (SCB)
- short circuit to ground (SCG)
- open load (OL)
- Overtemperature detection (OTW)

Parameter	Min	Typ	Max	Unit
Output current	350			mA
Leakage current (in standby)			10	uA
Clamping voltage		55		V

POWER STAGES

The CY329 comprises 8 power stages:

- 6 low side power stages at [OUT_LS1 ... OUT_LS6]
- 1 low side starter power stage at [OUT_LS7]
- 1 high side starter power stage at [OUT_HS8]

The power stages are controlled via the MSC interface. Additionally, the [OUT_LS1...3] stages can **directly be controlled by the wake-up pins** [WAK1...3].

The [OUT_LS1...6] low side power stages as well as the [OUT_LS7] and [OUT_HS8] starter power stages can be configured to have a **delayed shut-down behavior**.

The power stages provide **short circuit detection** with **current limitation** in active mode (short to battery for LS, short to GND for HS). When the power stages are disabled, the outputs are monitored regarding **short circuit or open load** (short to GND for LS, short to battery for HS). These diagnostic features are tested during start-up by means of an **internal self-test**.

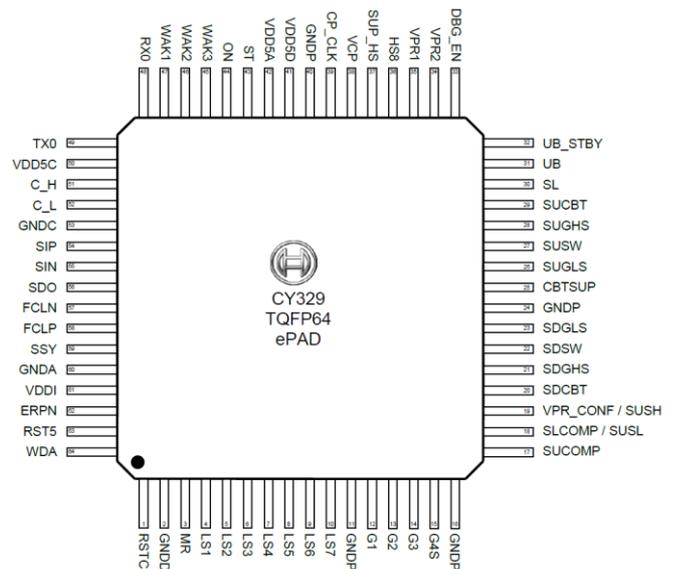
The stages are monitored for **overtemperature**. The supply of the HS switch, [SUP_HS], is monitored for **overvoltage** and **undervoltage** conditions.

Parameter (valid vor both LS and HS)	Min	Typ	Max	Unit
R _{on} @ 25°C		720		mΩ
R _{on} @ 150°C		1300		mΩ
Switch on/off delay			10	us
Switch on/off slew rates		4		V/us
Clamping voltage		55		V

SAFETY (ISO26262)

The CY329 is designed for use in safety relevant systems up to ASIL C(D). It provides various safety related features for self and system monitoring. The complete safety concept has to be worked out based on individual system requirements.

PIN ASSIGNMENT



System Basis Chip CY329

PIN DESCRIPTION

Pin	Pin name	Description
1	RSTC	Core reset input/output
2	GNDD	Ground digital
3	MR	Low side power stage for main relay control
4	OUT_LS1	Low side power stage #1
5	OUT_LS2	Low side power stage #2
6	OUT_LS3	Low side power stage #3
7	OUT_LS4	Low side power stage #4
8	OUT_LS5	Low side power stage #5
9	OUT_LS6	Low side power stage #6
10	OUT_LS7	Low side power stage #7 (with starter functionality)
11	GNDP	Ground power
12	G1	Output of sensor supply #1
13	G2	Output of sensor supply #2
14	G3	Output of sensor supply #3
15	G4S	Input for external voltage tracker
16	GNDP	Ground power
17	SUCOMP (SDCOMP)	Input for step-up compensation network (VPR) In buck-only mode input for step-down compensation network.
18	SLCOMP (SUSL)	Input for step-down compensation network (VPR) Lower shunt connector for step-up current limitation in dual-coil configuration (SUSL)
19	VPR_CONF (SUSH)	Config. of VPR current limitation (high/low level) Upper shunt connector for step-up current limitation in dual-coil configuration (SUSH)
20	SDCBT	Step-down bootstrap capacitor
21	SDGHS	Gate of step-down highside-MOSFET
22	SDSW	Step-down switching node
23	SDGLS	Gate of step-down lowside-MOSFET
24	GNDP	Ground power
25	CBTSUP	Bootstrap for VPR regulator
26	SUGLS	Gate of step-up lowside-MOSFET
27	SUSW	Step-up switching node
28	SUGHS	Gate of step-up highside-MOSFET
29	SUCBT	Step-up bootstrap capacitor
30	SL	Lower shunt connection of VPR step-down current limitation
31	UB (SH)	Battery pin
32	UB_STBY	Battery pin (depending on configuration)
33	DBG_EN	Debug mode input
34	VPR2	VPR voltage (input for VPR regulator, supply for VDD5x, Gx)
35	VPR1	VPR voltage (Supply for VDD5x, Gx)
36	OUT_HS8	High side power stage (with starter functionality)
37	SUP_HS	Supply pin for high side power stage
38	VCP	Charge pump voltage

Pin	Pin name	Description
39	CP_CLK	Charge pump clock signal for operating external charge pump
40	GNDP	Ground power
41	VDD5D	Output of 5V power supply VDD5D linear regulator
42	VDD5A	Output of 5V reference supply VDD5A linear regulator
43	ST	Output of filtered ON status
44	ON	ON pin input for wakeup via T15 (ignition)
45	WAK3	WAK3 input for wakeup via WAK event
46	WAK2	WAK2 input for wakeup via WAK event
47	WAK1	WAK1 input for wakeup via WAK event
48	RX0	Receiver output of CAN receiver
49	TX0	Transmitter input for CAN driver
50	VDD5C	5V supply for CAN (connect to VDD5D on pcb)
51	C_H	CAN bus HIGH
52	C_L	CAN bus LOW
53	GNDC	CAN ground
54	SIP	HIGH portion of differential MSC slave in signal
55	SIN	LOW portion of differential MSC slave in signal
56	SDO	MSC slave data out output
57	FCLN	LOW portion of differential MSC clock signal
58	FCLP	HIGH portion of differential MSC clock signal
59	SSY	MSC slave select signal input
60	GND A	Ground analog
61	VDDI	3.3V internal supply voltage
62	ERP N	Error-pin input/output
63	RST5	Peripheral reset input/output
64	WDA	Monitoring module output

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