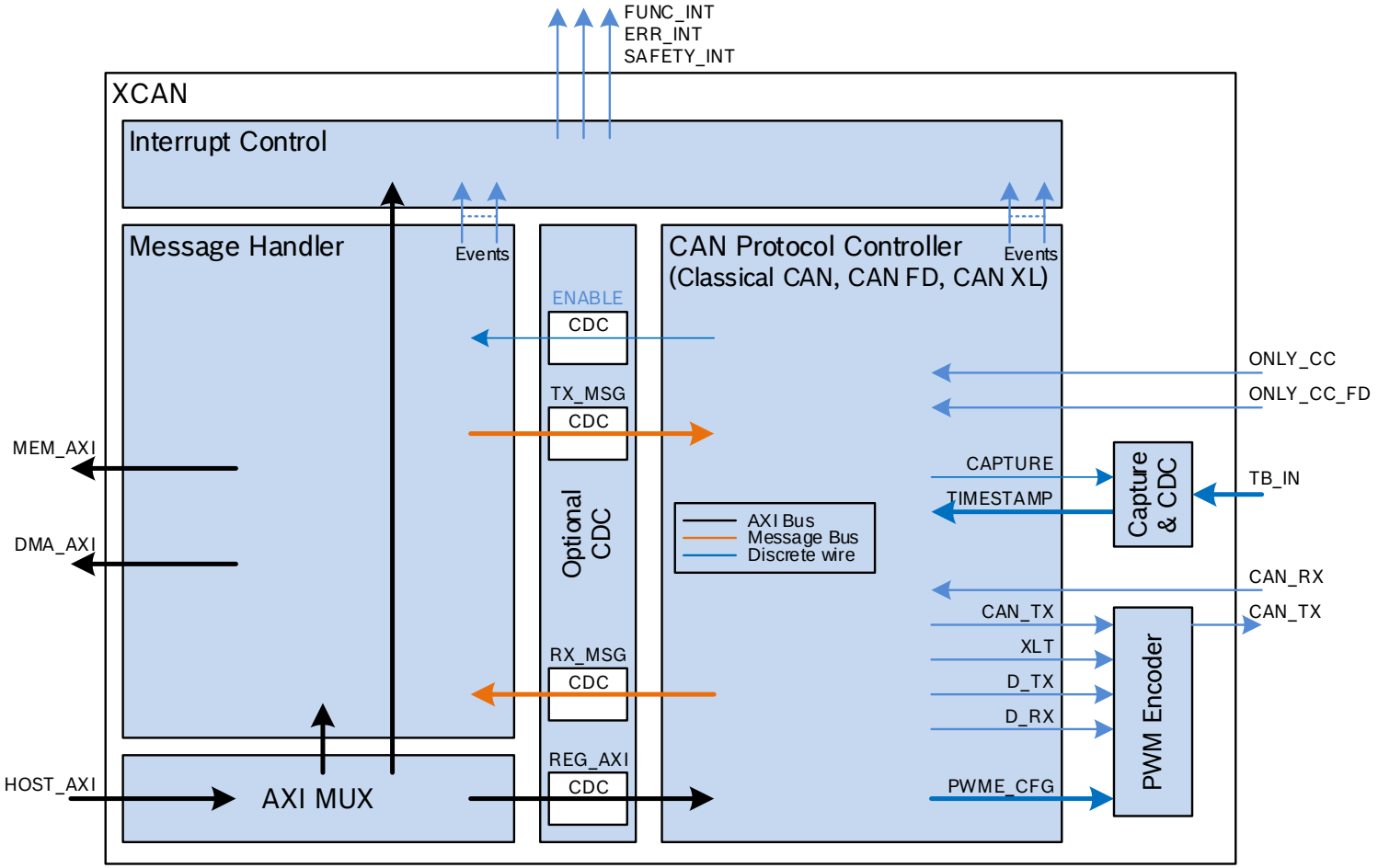
X_CAN IP-MODULE OVERVIEW

BOSCH

X_CAN IP-Module Overview

- Support of Classical CAN, CAN FD
- Full support of CAN XL protocol with payloads up to 2048 bytes
- Small local memory (4 kbytes) considering 128 RX filter elements, 256 value/mask pairs, all RX/TX FIFO queues, all TX priority queue slots
- Message storage in system memory
- Internal DMA engine, X_CAN acts as DMA master for message handling
- AXI4 DMA system, 32bit bus interface, max. burst size of 8x32bit
- Low CPU impact, any accesses to/from the system memory are done using the internal DMA engine (less interrupts)
- 8 RX FIFO queues, each with up to 1024 messages
- 8 TX FIFO queues, each with up to 1024 messages
- 1 TX priority queue, with up to 32 slots, configurable by SW
- RX filtering with up to 255 filter elements
  (2 comparisons per filter element, up to 256 value/mask)
- TX filtering capabilities to support security
- 64-bit Timestamps from external Timebase supported
- Privileged accesses to protect configuration and RX/TX filtering (optional)

X_CAN IP-Module Overview
Block Diagram



X_CAN IP-Module Overview
X_CAN Interface

Signal	Dir	Function
HOST_AXI	I/O	RD/WR access to config/control/status registers
DMA_AXI	I/O	DMA Interface for message transfer between X_CAN and System RAM
MEM_AXI	I/O	Interface to local Message RAM
FUNC_INT	O	Functional Interrupt
ERR_INT	O	Error Interrupt
SAFETY_INT	O	Safety Interrupt
CAN_RX	I	CAN receive input from transceiver
CAN_TX	O	CAN transmit output to transceiver
TB_IN	I	Time Base Input from external counter for 64-bit time stamping
ONLY_CC_FD	I	If fixed to '1' only Classical CAN and CAN FD operation enabled
ONLY_CC	I	If fixed to '1' only Classical CAN operation enabled

X_CAN IP-Module Overview
X_CAN is DMA Master

- Advantages
  - Limits required local RAM size to 4 kbyte
    - Local RAM buffers part of RX/TX messages during transfer from/to system memory
    - Local RAM holds acceptance filter elements
    - Local RAM holds a copy of active descriptors for DMA transfer from/to system memory
  - RX/TX data stored in system memory
    - All data handled in system memory
    - No extra transfers from/to local RAM to be initiated by CPU
    - Reduced interrupt load

X_CAN IP-Module Overview
Timeline

- Revision 1.0.0 — Q2/2022
  - CAN XL implemented according to CiA610-1 V1.0.0 (Nov. 2021)
  - Conformance Tested for Classical CAN and CAN FD according to ISO 16845-1:2016
- Revision 1.0.0XL — depending on availability of CAN XL CT
  - Conformance Tested for Classical CAN, CAN FD, and CAN XL
- Licensing conditions available at Bosch AE

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