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MathAcceleration IP

IP TechDay
We enable possibilities

DFA – DATAFLOW ARCHITECTURE

- DIGITAL HARDWARE IP -

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Introduction

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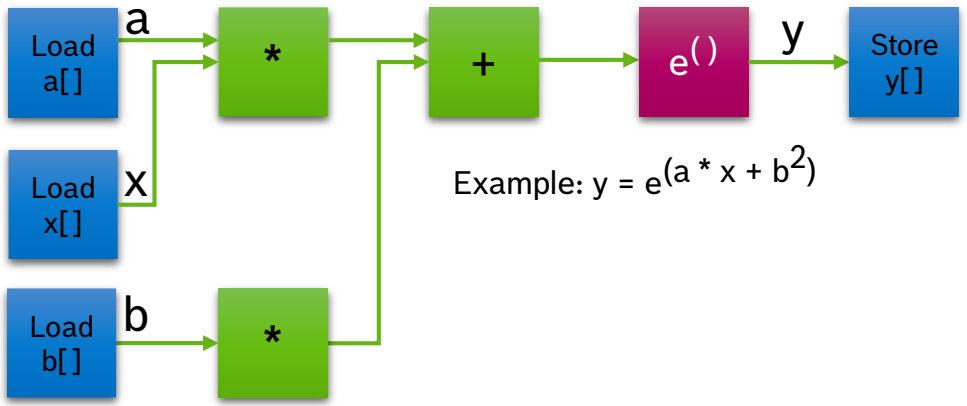
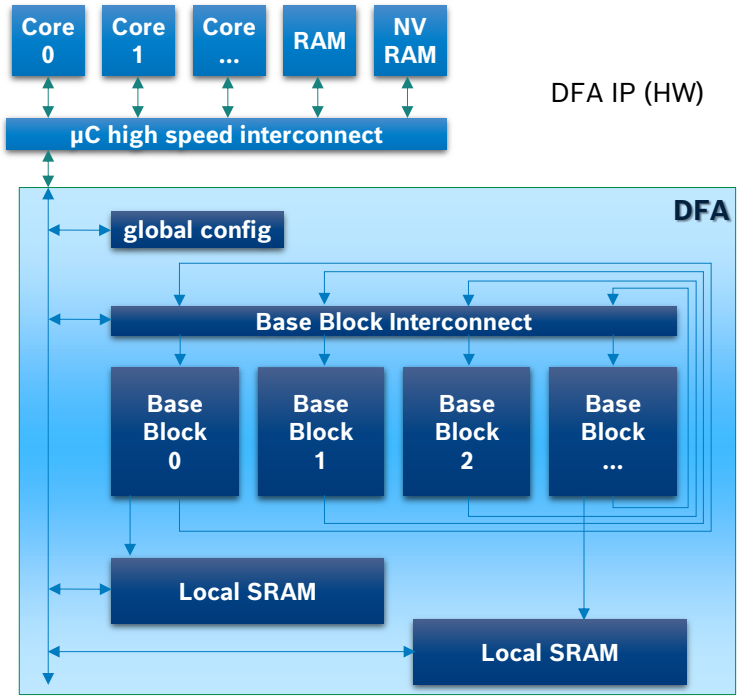
- Native dataflow execution in hardware
- Major advantages over SIMD*) based architectures
- Usage of coarse-grained “Base Blocks” (load, store, MAC, exp, trigon., …)

dataflow graph (math)



mapping:
math → HW

DFA IP (HW)



*) SIMD = Single Instruction Multiple Data

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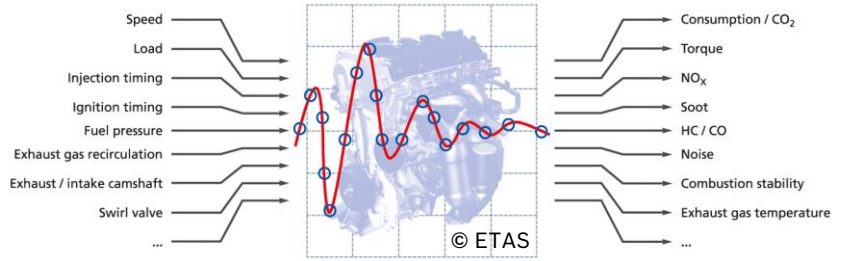
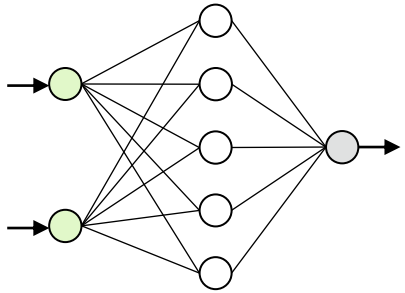
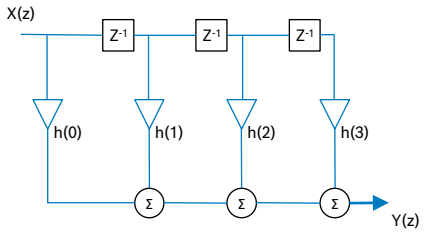
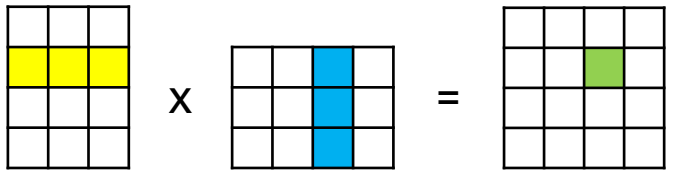
Algorithms supported

- Machine Learning, AI
  - Neural Networks (MLP, CNN, ...)
  - Gaussian RBF / Bayes regression (different types)
  - Support Vector Machine (Polynomial, Gaussian, ...)
- Signal Processing
  - (i)FFT, FIR, IIR
- Control Theory
  - Matrix and vector operations
- Control Theory (planned, next gen)
  - Linear equation solver, Matrix inversion, Cholesky
- Physical Equations
- Combinations of algorithms









Benefits

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Performance	• Compute power ~10x above multicore µC, to offload SW cores
Low Cost	• Very small footprint (e.g. 28nm silicon: 1mm²) • Low power consumption (housing)
Accuracy	• float32 / float64 (IEEE)
Embedded	• Embedded Algorithms • Fast response time
Scalability	• Small sensors, embedded computing, radar, intelligent sensors, ADAS
Safety	• Up to ASIL-D

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Status

µC Integration

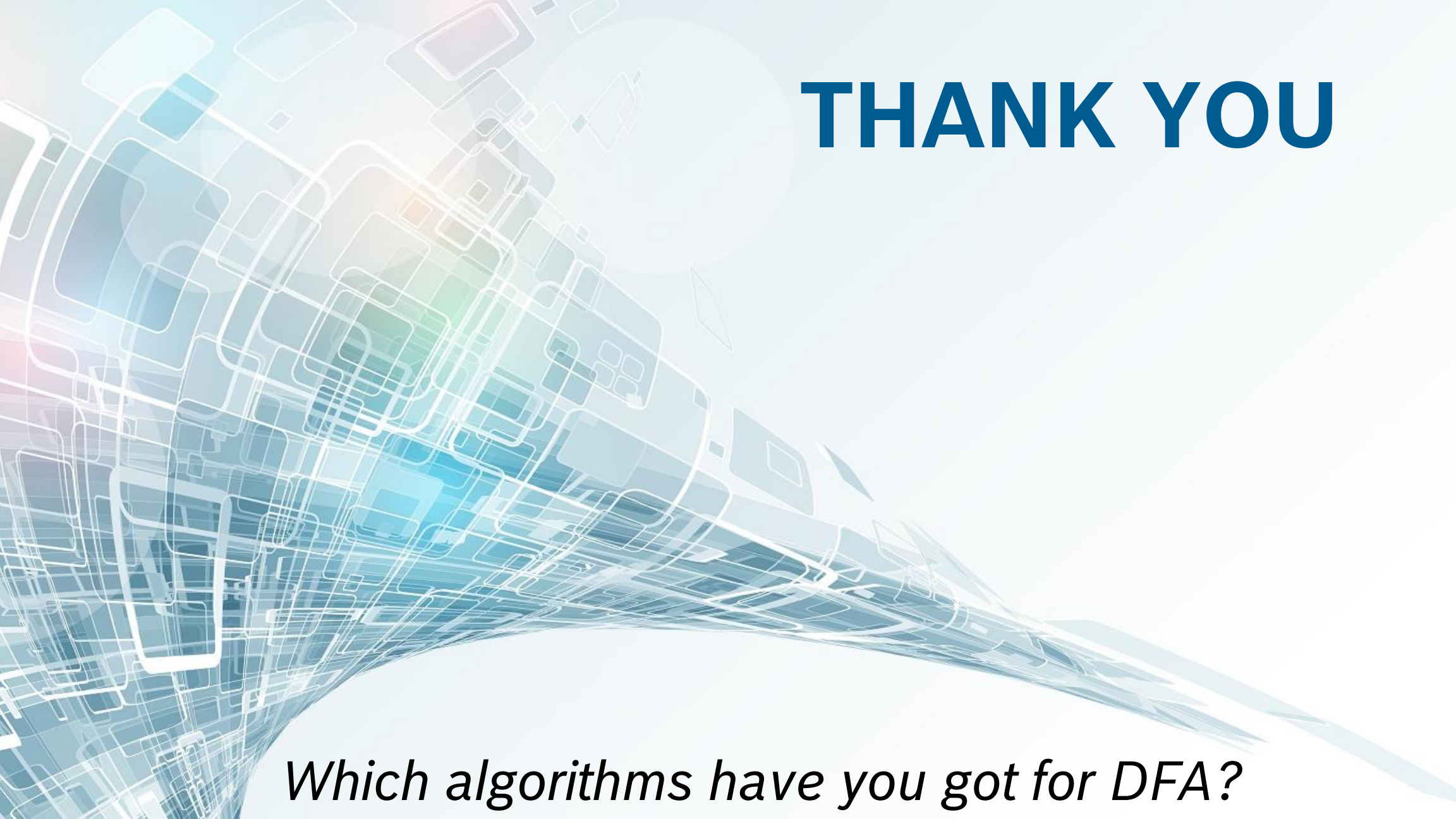
- Several µC available from different semiconductor vendors, others will follow
- Different DFA architectures under investigation (e.g. for smart sensors, Radar, DNN)

SW Driver

- AUTOSAR-compliant series driver 07/2023 for 1st algorithm
- Priority based scheduling
- Switching different algorithms at kHz-rate

Prototyping

- Testboards, SystemC model, FPGA emulation
- Debugger support


THANK YOU
Which algorithms have you got for DFA?