



# **X\_CAN IP-Module Overview**

Sunderdiek, ME-IC/PRM-IP, October 2025

# IP business @ Bosch Mobility Electronics

## IP Portfolio



### I/O Processing IP

#### GTM IP Gen 4



... realtime oriented I/O co-processor  
(aka "Timer")

- A scalable timer solution for ...
  - digital input data processing (e.g. sensor data)
  - digital output data generation (e.g. PWMs for actor control)
- Integrated multi-threaded RISC cores for real-time oriented control loops
- Generic architecture to address multiple domains
  - Powertrain (combustion & electric)
  - Chassis and Body applications
  - Inverter, PFC,
  - ...

### Communication IPs


#### CAN IPs



... Controller Area Network IPs

- **X\_CAN IP**
  - Triple-protocol support: \*1
    - Classical CAN, CAN FD and **CAN XL (new)** and CAN FD light commander
  - Active DMA support
  - Bitrates up to 20 Mbit/s
  - Payload up to 2048 byte
- **M\_CAN IP**
  - Dual-protocol support: \*1
    - Classical CAN and CAN FD and CAN FD light commander
  - Bitrate up to 8 Mbit/s
  - Payload up to 64 bytes

- **XS\_CAN IP**
  - Small gate count
  - Triple-protocol support:
    - Classical CAN, CAN FD and **CAN XL (new)**
  - Bitrates up to 20 Mbit/s
  - Payload up to 2048 byte
  - CAN FD light Commander up to 8Mbit/s (**new**)

- **FDLR\_CAN IP** 
  - CAN FD light responder IP
  - For Responder Nodes, MCU less
  - Bitrate up to 8 Mbit/s
  - Payload up to 64 bytes

#### CAN protocol licensing

- CAN FD (light) protocol license
- CAN XL protocol license

\*1, CAN FD light Commander up to 1 Mbit/s

### Accelerator IP

#### DFA IP Data Flow Architecture

... HW based accelerator for advanced mathematical algorithms

- Ready for AI & ML (Artificial Intelligence, Machine Learning)
- Data-based modeling, signal processing, control theory, physical equations
- Enabler for new compute-intensive functions e.g. novel features + legal regulations like EU7, OBM

#### Computer Vision IP Gen 2

... comprehensive set of computer vision processing elements

- Optical Flow
  - Optical flow field estimation
  - Native 12MPix input image resolution support
  - Nearly one flow vector per pixel
  - Camera's ego-motion estimation
- Stereo Disparity module
- Classifier Engine
- Structure from Motion Detection

# CAN XL – Next Step in CAN Evolution

## ISO: Standardization Published



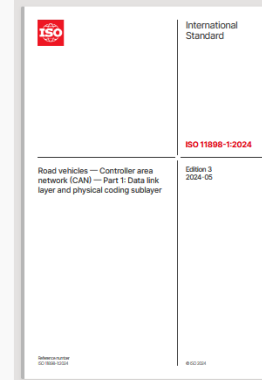
### ISO11898-1:2024

#### Contains all CAN Protocols

- CAN CC (unchanged)
- CAN FD (unchanged)
- CAN XL
- CAN FD light responder

#### Status

Published on  
May 24<sup>th</sup>, 2024



### ISO 11898-1:2024

Road vehicles — Controller area network (CAN)  
Part 1: Data link layer and physical coding sublayer

Published (Edition 3, 2024)

Source: ISO web site <https://www.iso.org/standard/86384.html>



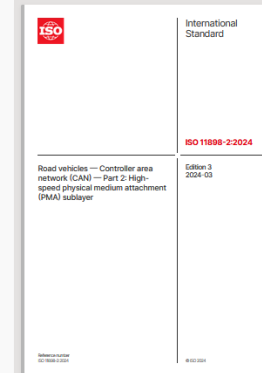
### ISO11898-2:2024

#### Contains all CAN Transceivers

- HS-CAN (unchanged)
- CAN FD (unchanged)
- CAN SIC
- CAN SIC XL

#### Status

Published on  
March 22<sup>nd</sup>, 2024



### ISO 11898-2:2024

Road vehicles — Controller area network (CAN)  
Part 2: High-speed physical medium attachment (PMA) sublayer

Published (Edition 3, 2024)

Source: ISO web site <https://www.iso.org/standard/85120.html>

# CAN XL – Next Step in CAN Evolution

## Superior up to 20 Mbit/s network solution



IP available

Broad availability in nextGen  $\mu$ Cs

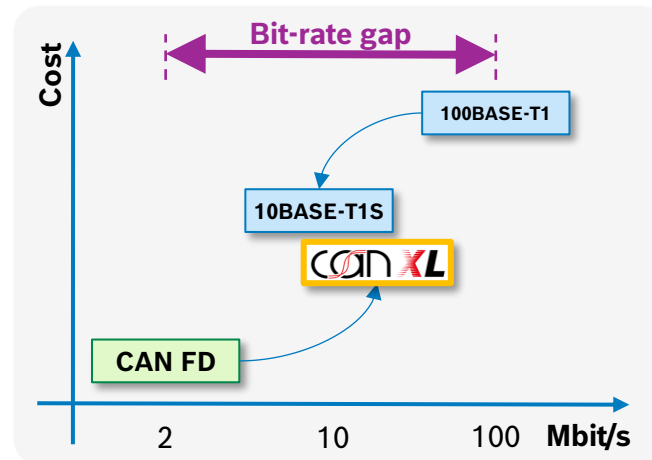
### Target / Motivation



Provide a superior  $\leq 20$  Mbit/s CAN solution with respect to

- Price (Transceiver, Pins, Cabling, ...)
- Safety and Security
- Enables SOA (Service Oriented Architecture)
- Quality of Service

Preserve CAN properties: Arbitration, robustness, long stubs, ...



### Compatibility of CAN FD and XL enables ...



- Incremental upgrade path  
➔ larger acceptance (re-use of CAN / CAN FD knowhow and equipment)
- E/E Architecture design freedom: “mixed FD/XL” or “XL only” networks:
  - “XL only” networks up to 20 Mbit/s
  - “mixed” networks limited to 8 Mbit/s (e.g. XL 8 Mbit/s, FD 2 Mbit/s)

### Key Success Factors

- 1) **Cost Optimal E/E Architectures**  
Single bus for 3 types of traffic (CAN FD, CAN XL and Ethernet)
- 2) **Bit rate up to 20 Mbit/s**  
Compatible with wide range of transceiver (HS-CAN, FD, SIC, SIC XL)
- 3) **Large payload size (1 .. 2048 bytes)**  
enough space for any application
- 4) **Ethernet Tunneling**  
allows use of TCP/IP, SOME/IP, etc.
- 5) **Incremental upgrade**  
Allows CAN FD and CAN XL on the same network (up to 8 Mbit/s)
- 6) **Scalable**  
flexible tradeoff between cost, speed and network complexity
- 7) **Broad availability**  
majority of nextGen automotive  $\mu$ Cs

# IP business @ Bosch AE

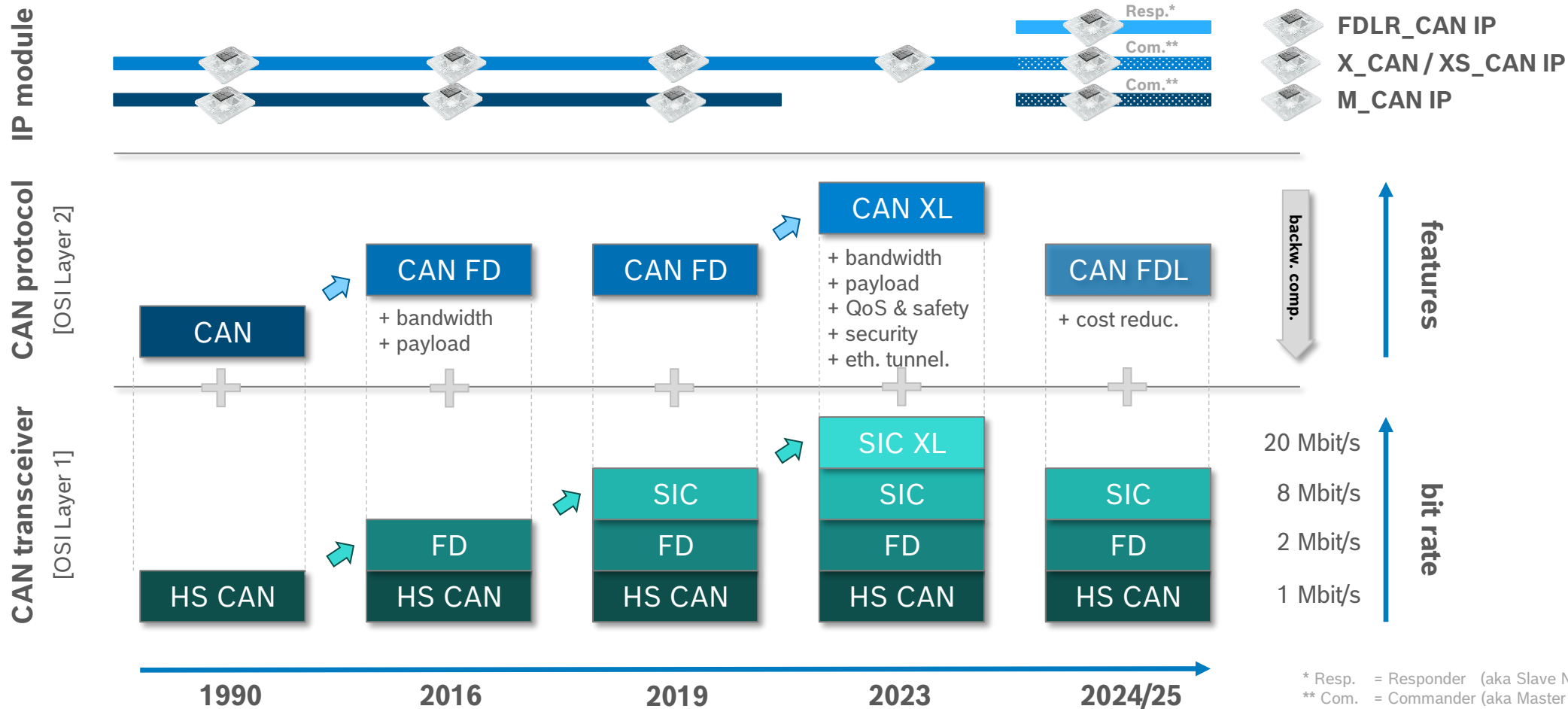
## CAN roadmap

CAN

CAN<sup>FD</sup>

CAN<sup>FD</sup> Light

CAN<sup>XL</sup>



## FEATURES

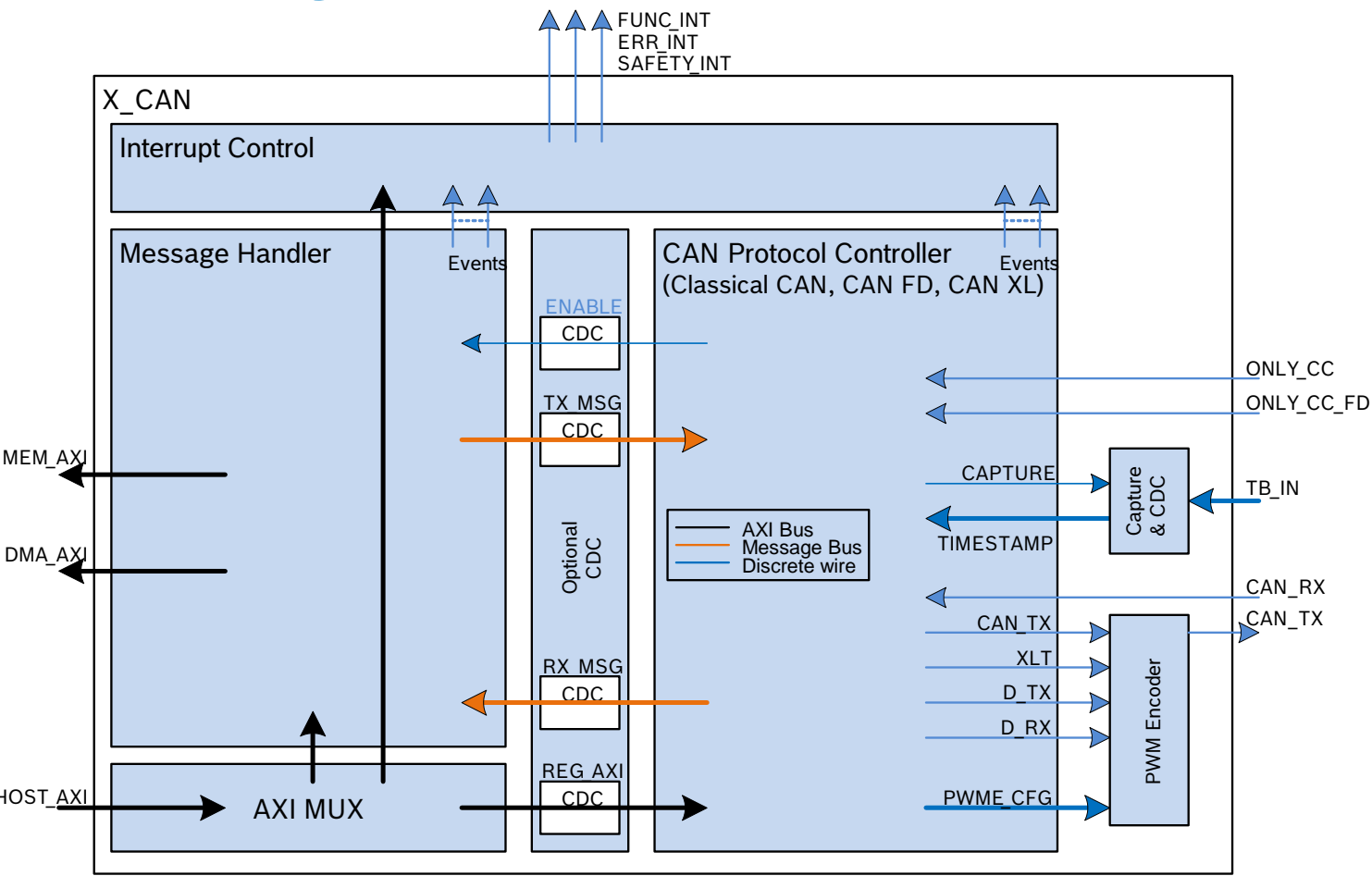
- Support of CAN CC, CAN FD, and CAN XL
  - Conform with ISO11898-1:2024
- Full support of CAN XL protocol
  - Up to 20Mbit/s and up to 2048 bytes
- Small local memory
  - approx. 4 Kbytes for up to 255 filter elements
- Internal DMA engine, XCAN acts as DMA master for message handling
  - Message storage in system memory
  - Low CPU impact, any accesses to/from the system memory are done using the internal DMA engine (less interrupts)
- 8 RX FIFO queues, each with up to 1024 messages
- 8 TX FIFO queues, each with up to 1024 messages
- 1 TX priority queue, up to 32 slots, configurable by SW
- 255 RX filters on the first 8 byte of a frame (e.g., CAN XL header and AF)
- TX filtering capabilities to support security
- Privileged accesses to protect configuration and RX/TX filtering (optional)
- 64-bit Timestamps from external Timebase
- ASIL D capable with external measures

## FEATURES

- AXI interface compliant to AMBA 4 ARM Ltd protocol
  - AXI4-Lite slave interface (HOST\_AXI)
  - AXI4 master DMA interface (DMA\_AXI)
  - AXI4 master Local Memory interface (MEM\_AXI)
- CAN Error Logging
- Fault Injection Module
- Programmable loop-back test mode
- Multiple X\_CAN can share the same Local Memory
- Maskable module interrupts with three categories: Functional, Functional Error and Safety
- Three clock domains (HOST, CAN, TIMEBASE)
- Power-down support

# X\_CAN Overview

## Block diagram (simplified)



Signal	Dir	Function
HOST_AXI	I/O	RD/WR access to config/control/status registers
DMA_AXI	I/O	DMA Interface for message transfer between XCAN and System RAM
MEM_AXI	I/O	Interface to local Message RAM
FUNC_INT	O	Functional Interrupt
ERR_INT	O	Error Interrupt
SAFETY_INT	O	Safety Interrupt
CAN_RX	I	CAN receive input from transceiver
CAN_TX	O	CAN transmit output to transceiver
TB_IN	I	Time Base Input from external counter for 64-bit time stamping
ONLY_CC_F D	I	If fixed to '1' only Classical CAN and CAN FD operation enabled
ONLY_CC	I	If fixed to '1' only Classical CAN operation enabled

Glossary:

- CDC - Clock Domain Crossing

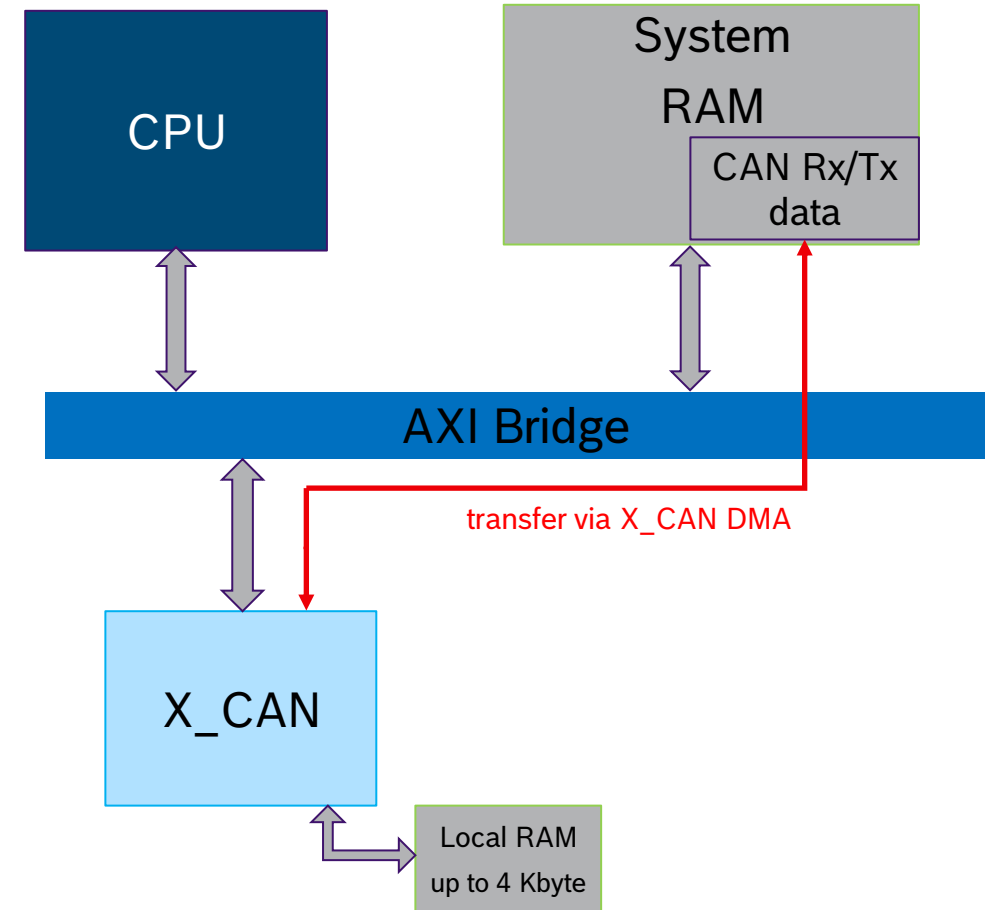


# X\_CAN Overview

## X\_CAN is DMA Master

### Advantages

- RX/TX data stored in system memory
  - All data handled in system memory
  - No extra transfers from/to local RAM to be initiated by CPU
  - Reduced interrupt load for processor core
- Only small local RAM required (up to 4 Kbyte)
  - Local RAM holds acceptance filter elements
  - Local RAM holds active descriptors for DMA transfer to system memory



# X\_CAN Overview

## Timeline & Deliverables



### Revision 1.1.0

Available

Deliverables include:

- VHDL Source Code
- User Manual (programmer's view)
- Module Integration Guide (designer's view)
- FMEDA
- Safety Manual
- Functional Safety assessment certificate
- Conformance Test Report for CAN and CAN FD
  - Passed in June 2022

Licensing conditions available at Bosch AE

Please see: <https://www.bosch-semiconductors.com/ip-modules/can-protocol-license/>



### Revision 1.1.0

### CAN XL Conformance tested

depending on availability of CAN XL CT

Planned for Q1/2026

Conformance Tested for Classical CAN,  
CAN FD, and CAN XL

# X\_CAN Overview

## IP Delivery content and Service

- The X\_CAN package include:
  - xcan\_readme.txt, User manual, Integration guide, both as pdf and as word document
  - Excel Sheet for calculation memory latency and min. Host clock,
  - Safety Case documents:
    - Safety Manual, Safety Certificate, DFA (Dependent Failure Analysis), DIA (Development Interface Agreement), FMEDA (Failure modes, effects, and diagnostic analysis)
  - Verification report, Verification Plan Summary, Spyglass configuration files, constraint file for synthesis and IP-XACT XML file, synchronizer list.
- Service include:
  - Free updates for the X\_CAN IP, Errata, Testbench
  - AppNote: Transmission **Transmission and Reception Handling with FIFO Queue + SW examples**
  - Free Technical support during integration
  - Free Technical support during usage of the X\_CAN IP, e.g., bring up / debugging for CAN CC/FD/XL messaging