

A decorative header featuring a series of overlapping, colorful triangles and polygons in shades of red, purple, blue, and green.

IP Tech Day 2026, Shanghai

GTM 5.0 Overview

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ME-IC/PAI, 16.09.2026

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GTM **Generic Timer Module**

GTM-IP

GTM – Generic Timer Module

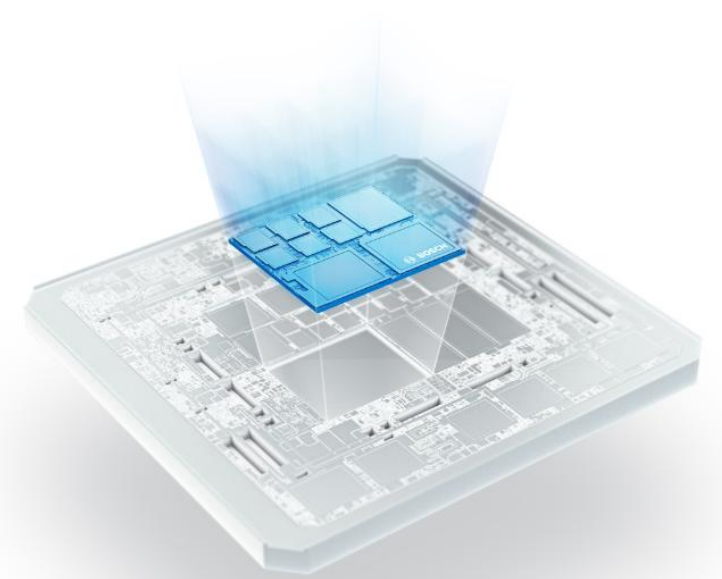
- **Timer functions:**

- capture digital input data (e.g., sensor signals)
- generate digital output data (e.g., PWM for actuator control)

- **GTM is a standardized, real-time I/O co-processor:**

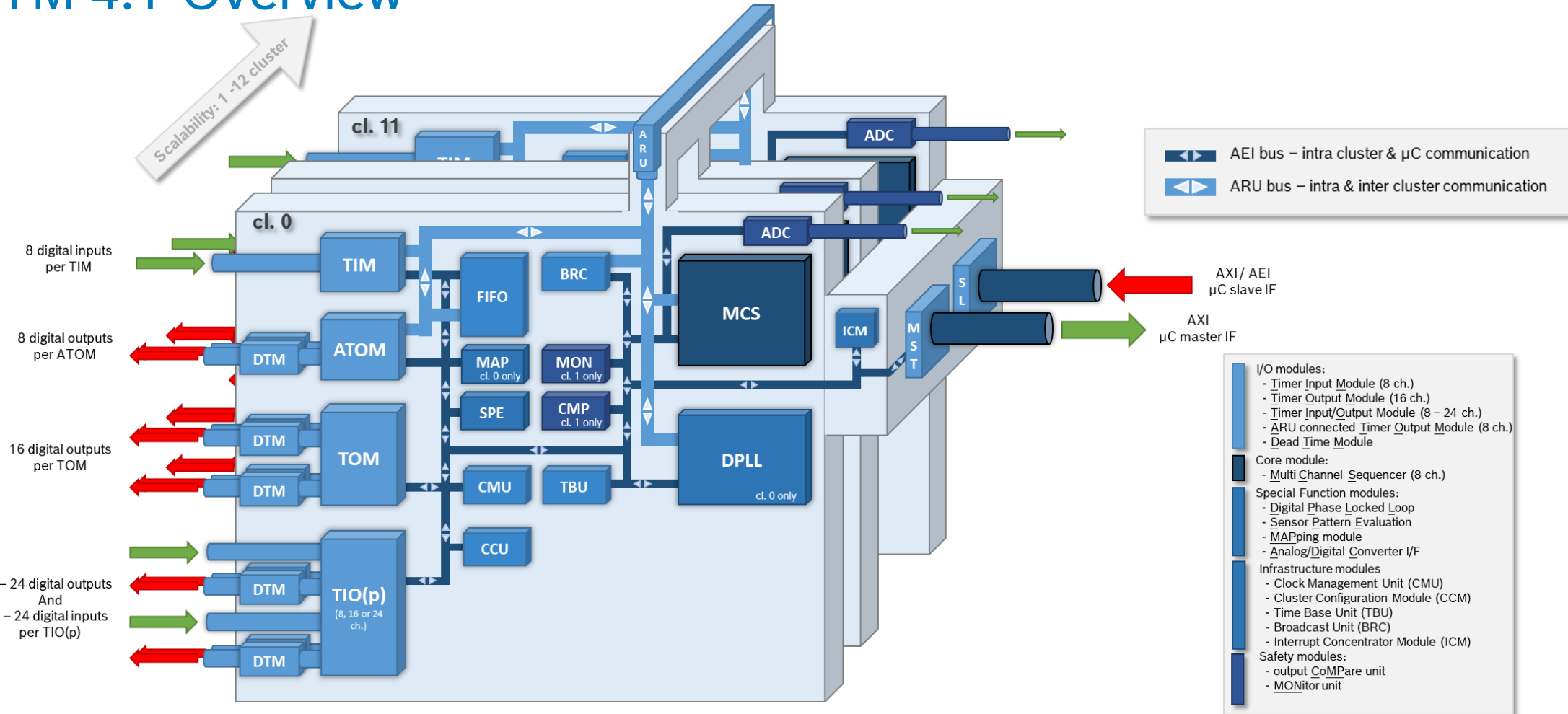
- processes digital input data (e.g., captures and processes sensor signals)
- generates digital output data (e.g., PWM for actuator control with closed-loop feedback)

- **Offloads time-critical I/O workloads from microcontroller cores to a specialized I/O co-processor with highly parallel thread-handling capabilities**



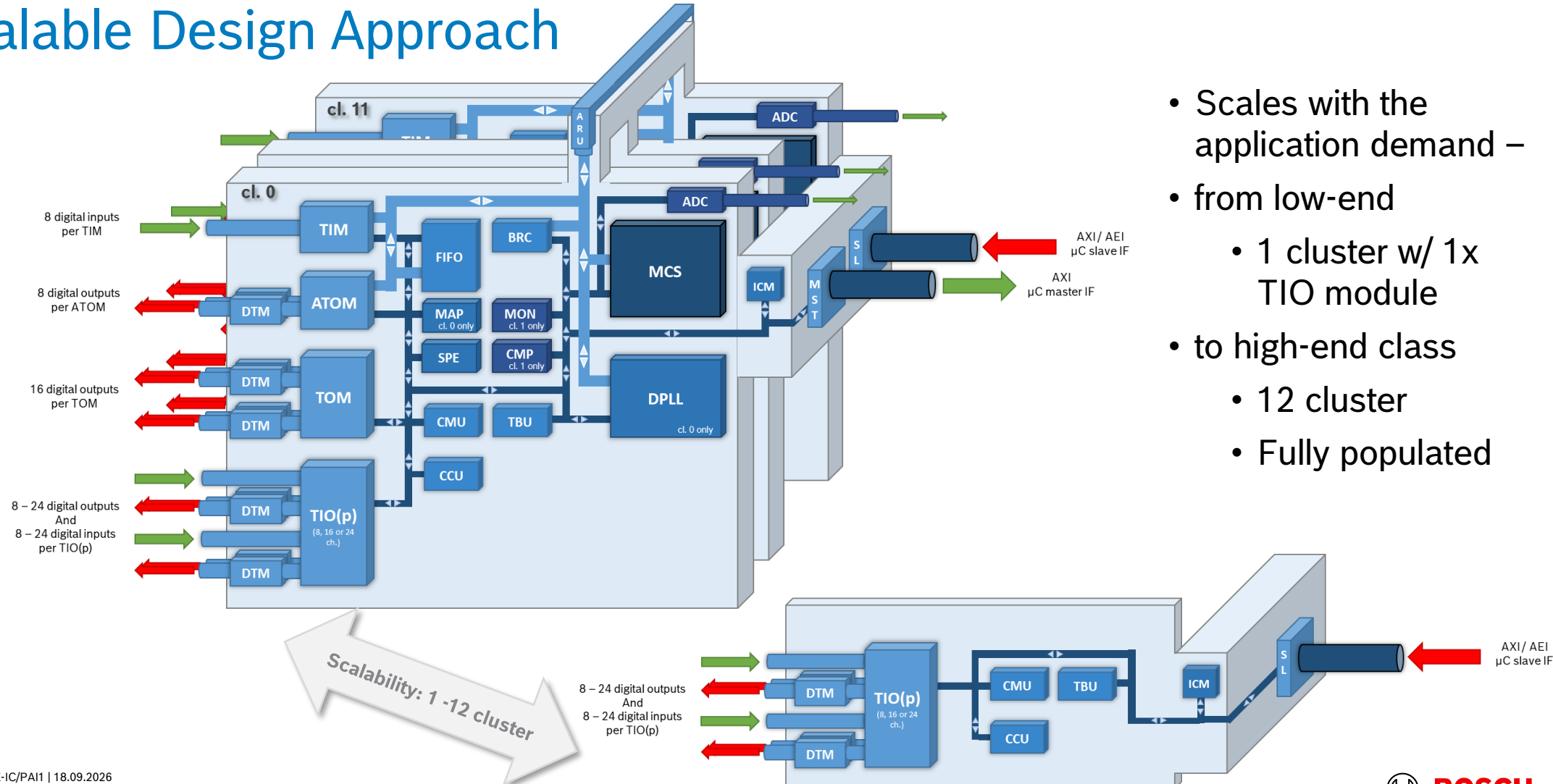
GTM-IP – IP

GTM 4.1 Overview



GTM-IP

Scalable Design Approach



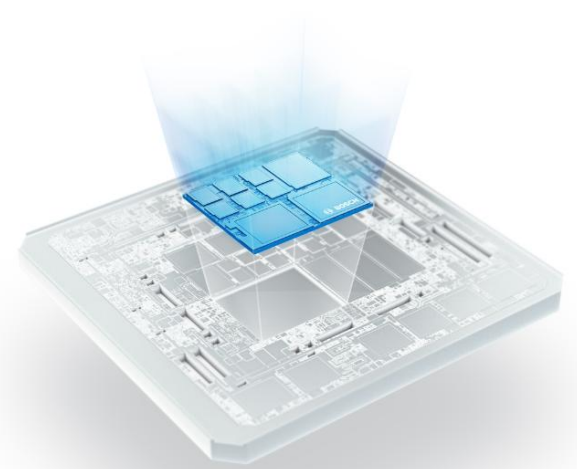
- Scales with the application demand –
- from low-end
 - 1 cluster w/ 1x TIO module
- to high-end class
 - 12 cluster
 - Fully populated

GTM-IP

GTM – Generic Timer Module

- **The Standard Timer for Applications**

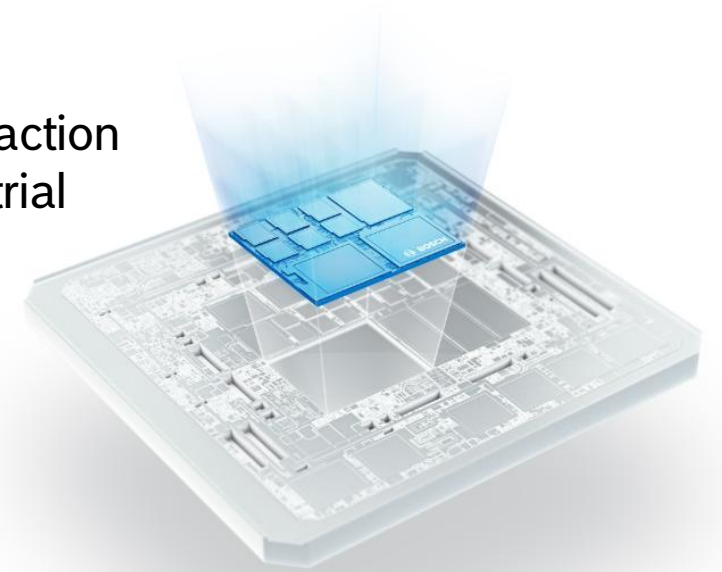
- 2008 – GTM development begins
 - Until then, only proprietary timer solutions were available
- The high cost of low-level I/O software development emerged as a major barrier to dual- and multi-sourcing
- Engine control units (ECUs) drove standardization
- Adoption quickly expanded to applications involving sensors and actuators—including body, chassis, and EV systems—and beyond the automotive industry
- Now the de facto standard for automotive μ Cs
- High-volume of SoCs with GTM are in production



GTM

Benefits of the Generic timer Module

- **Common architecture across semiconductor platforms**
 - Enables software and application development independent of the selected MCU
- **Flexible, generic architecture**
 - Supports a broad range of applications, including powertrain, traction and chassis control, xEV, inverters, PFC converters, and industrial systems
- **Growing ecosystem**
 - Enables a rich ecosystem of development tools and compilers
- **Benefits the entire automotive industry**
 - Reduces application development costs



GTM

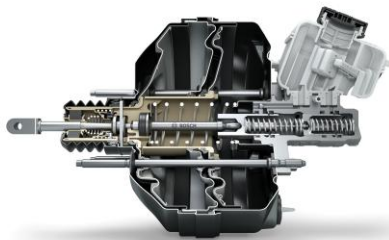
GTM supports applications throughout the vehicle



Steering



Cooling fan



Braking



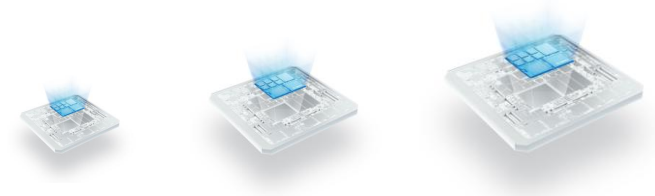
Charger &
converter



Combustion engine

GTM-IP – Overview GTM Gen 1 – Gen 4

Delivered device configuration 2010 - 2025



GTM IP Deliveries

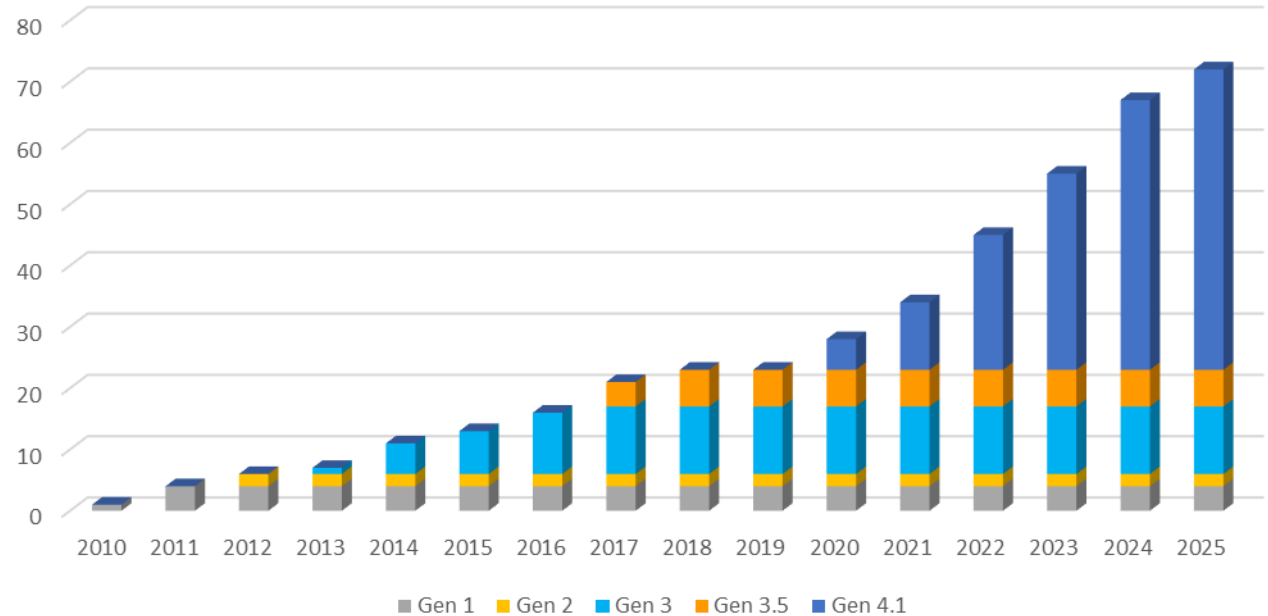
First GTM IP (Gen 1) delivered in 2010

Meanwhile more than 50 different configurations delivered to multiple semiconductor vendors

Delivery of GTM IP Gen 4 starting in 2020/21

GTM Gen 4.1 devices dominating the list with more than Gen 3/3.5 in less than 2 years

Delivered GTM configurations
(by GTM IP Generation)



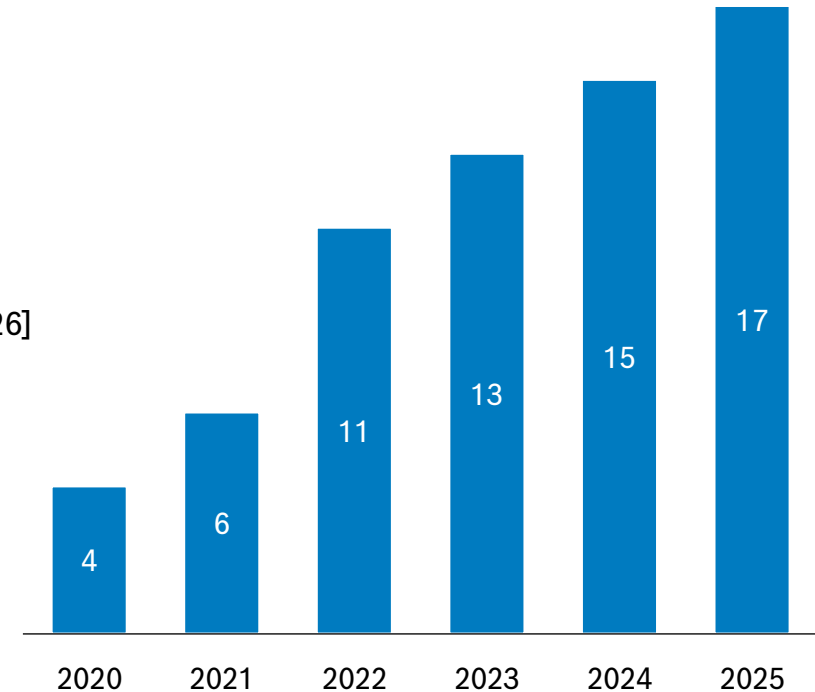
GTM-IP – Gen 4.1

Customers with GTM 4.1

Customer announcements:

- BinarySemi:
 - BS92360 (Sample)
- BYD Semi:
 - BS9523 (Sample)
- China Core:
 - CCFC3012PT,
 - CCRC4000 Series
- Chipsea:
 - CS32K776 (sample),
 - CS32K78x (in development)
- GigaDevice:
 - GD32A9 (in development)
- Infineon
 - [AURIX™– TC4x](#)
- NXP
 - [S32E2](#), [S32Z2](#)
- Renesas
 - [RH850/U2B](#)
- Semidrive
 - [E3620P](#)
- ST Microelectronics
 - [Stellar G](#), [Stellar P](#)
- StarPower:
 - StarDomain Family [samples 2026]
- ThinkTech:
 - Alioth TTA8 Series
- Tongxin Microelectronics
 - [THA6 gen2](#)
- XHSC:
 - XC27 SOPed;
 - XC3x in development

Number of GTM 4.1 licensee



Other customers are developing their products with the GTM.

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GTM 5

- **Motivation**
- **Overview**

GTM Gen 5

Motivation | Drivers of innovation

Electrification

Operating frequency – max. frequency & resolution of I/Os (increased GTM max. operating freq., modes of operation)
Higher compute performance – MCS with higher frequency and externally (low-latency path)
New PWM requirements – New emerging technology requires creating of complex waveforms

Ease of use

Regular structures & simplifications – new GTM top level design/architecture & inter-cluster resources

Interface perf.

Low latency access path to/from main CPU – updated internal GTM bus system
Industry standard interfaces – new top level interface concept - one AHB slave I/F per cluster

Virtualization

Isolation of global resources – introduction of central cluster and central resources
Freedom of interference – regular structures and resource access control

Safety

Improved safety mechanisms – e.g., freedom of interference,

Backwards comp.

Full support for legacy GTM applications (Gen 1 – Gen 4), No change of legacy modules

GTM Gen 5

New features - Overview



- New “Central Service Block” hosting all global resources
 - Legacy: CMU, TBU, ARU, ICM, BRC, MON, CMP
 - New: CCFG: Central Configuration Module
- New TOP level I/F per cluster
 - Each cluster can be accessed via a dedicated AHB I/F
- ABZ – New ABZ decoder
- FFI - Freedom of Interference
- New XTOM (Timer Output Module)
- Shared memory, semaphore
 - for the Central Service Block
- All GTM 4.1 errata fixed

GTM Gen 5

Backwards compatible to GTM Gen 1 to Gen 4.1

- All existing modules from GTM 4.1 will be the same as in GTM5
 - TOM, ATOM, TIM, TIO, DPLL, ...
 - Benefit: compatible to GTM Gen 1 to Gen 4.1
- In the new Central Service Block
 - Configuration modules will be moved from cluster 0 to the new Central Service Block
 - Configuration Modules are unchanged
 - Only change is a new address for CMU, TBU, BRC (Broadcast), ARU, CMP, MON, ICM
- AXI master I/F for the MCS
 - Same AXI master I/F
- Scalable as before
- Custom GTM 5.0 devices: define your needed GTM 5
- Standard GTM 5.0 devices: set of standard devices will be offered

GTM Gen 5

GTM 5 is developed with 2 Phases to enable fast delivery of Phase 1 features



GTM 5, first phase

- New “Central Service Block” hosting all global resources
 - CMU, TBU, ARU, .
- New TOP level I/F per cluster
 - Each cluster can be accessed via a dedicated AHB I/F
- ABZ – New ABZ decoder
- Freedom of interference
- All GTM 4.1 errata fixed

GTM 5, second phase

- New XTOM to address the need for electrification
- Shared memory, semaphore in the Central Service Block

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GTM Gen 5 - First Phase

GTM Gen 5

Phase 1

- Application need faster and parallel access of cluster registers
 - Improvement in the internal structure to achieve higher GTM frequency
 - AHB interface per cluster allows faster access of cluster registers
- Freedom of Interference – clusters can not interfere with other clusters
 - Several Application run on one GTM
 - X-IN-ONE
 - integration concept aiming to combine multiple powertrain functions, such as traction inverter, onboard charger (OBC), power conversion (DC/DC), high-voltage power distribution unit (HV PDU), vehicle control unit (VCU), battery monitoring system (BMS) and thermal management system
- Motor control
 - New AB decoder (2x channels, selectable)
 - designed to process quadrature signals (A/B/Z) from off-the-shelf incremental encoders.
 - GTM 4.1: Angle paths are optimized for DPLL crank/gear-wheel and MAP/SPE Hall use cases

Optimization of the GTM Structure

General and Top-Level topics

Frequency

- Target frequency: 500 MHz 20nm (w/ 4 cluster)

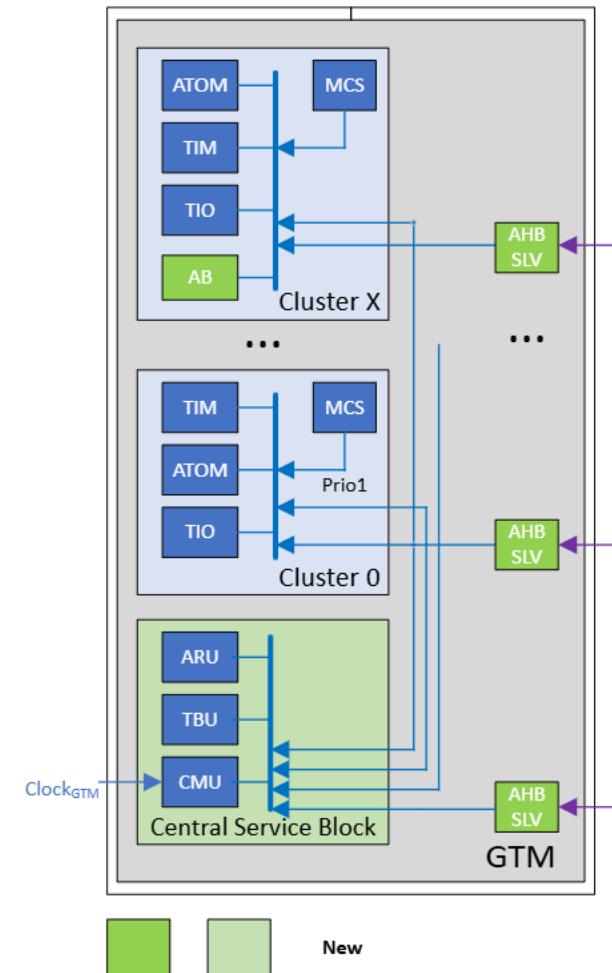
Bus I/F

- Keep AXI standard for GTM master
 - AXI master (MCS as masters), one I/F selectable per GTM config
- New AHB slave interface per cluster
 - no support for AEI/ anymore

Freedom of Interference FFI

ABD - AB Decoder

- New AB decoder, 2 channels ABZ



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GTM Gen 5 - Second Phase



GTM Gen 5

Phase 2

New requirements for timer:

- Driven by xEV

Application:

- Power Conversion
 - OBC On board Charger
 - Converter
 - Motor Drives
 - ...

New topologies for power conversion

- Matrix converter
- DAB Dual Active Bridge
- ...



**More information on the 2nd day in the presentation
“New functionalities for xEV with GTM5”**

GTM Gen 5

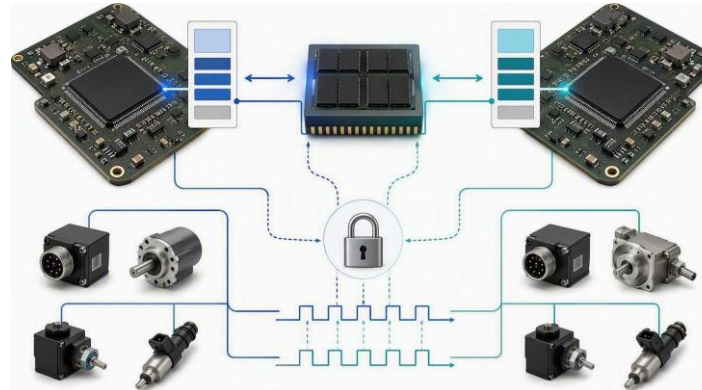
Phase 2

Shared Memory (SHM)

- General:
 - Sharing data between cores MCS and external,
- Motor Control
 - Lookup Tables (LUTs): Storing a sine/cosine or error-correction table in flash memory to linearize sensor non-linearities and improve precision
- Reduce involvement of SW interaction of main core

Semaphore Module SME

- Interrupt or periodic tick to safely signal a waiting task,
- coordinate precise periodic actions,
- prevent CPU-wasting busy-wait loops
- eliminate race conditions
- Trigger multiple XTOM at the same time



GTM Gen 5

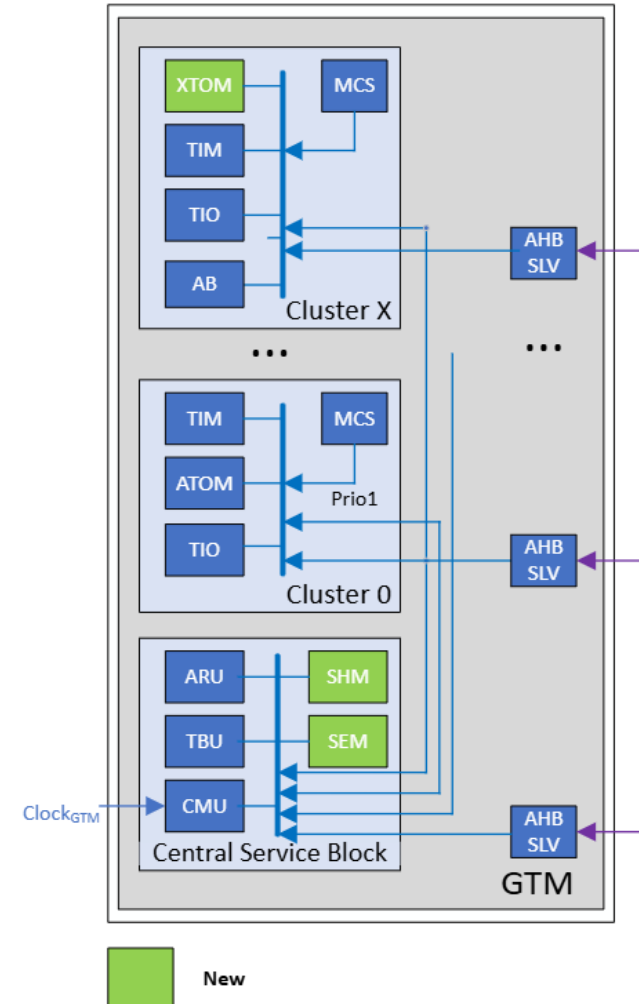
GTM 5.0, 2nd Phase = Phase 1 +

▪ New XTOM for advanced PWM generation

- 16 channels 16bit + 5-bit HRES
- New PWM Modes (e.g., Phase Shift)
- 3 edges (independent compare events)
- Synchronous atomic update of Parameter
- Flex of I/O Signal usage at DTM
- Up to 48 Channel sync (3x XTOM)
- Central Cluster (Enable sync)

▪ Inter-Core Communication – SHM & SME Extension

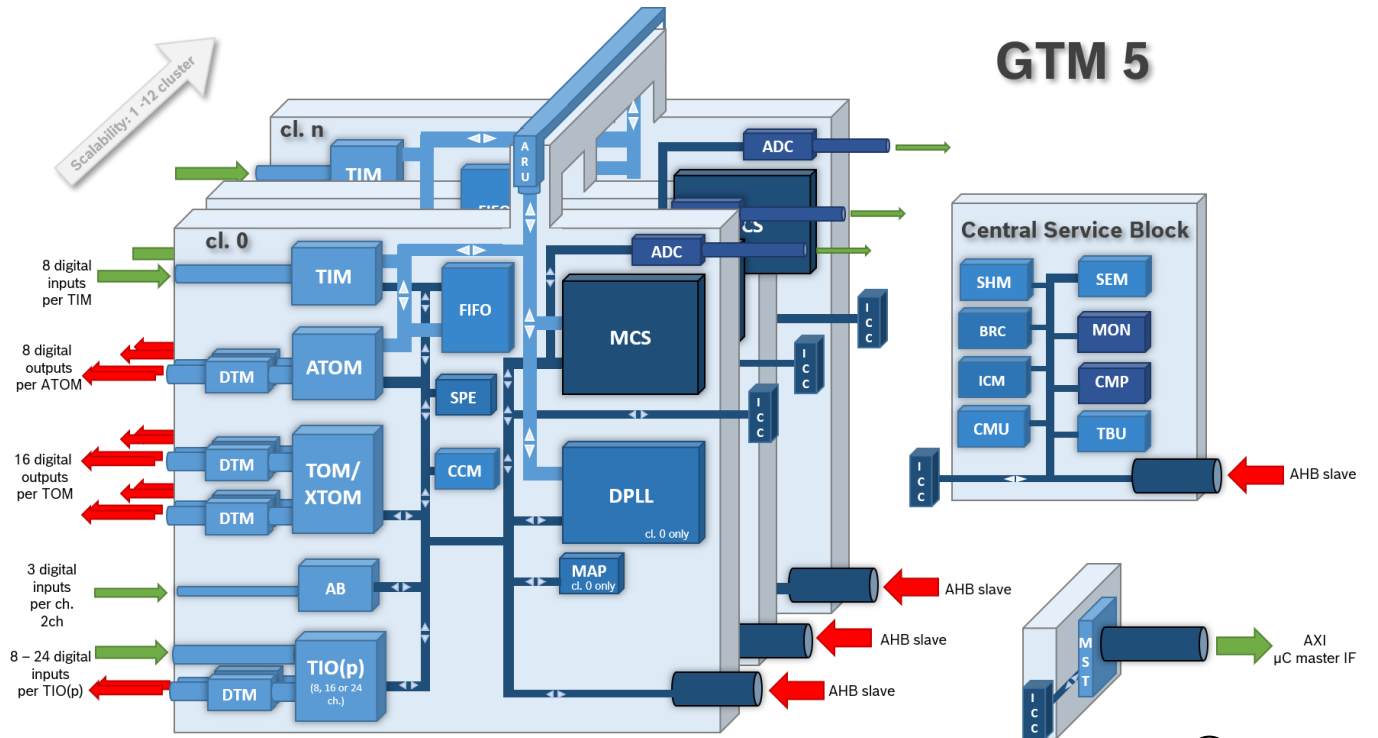
- Shared Memory (SHM) & Semaphore Module SME
 - located in Central Cluster
- Accessible by all bus masters (MCS, external cores)
- Allows interaction and data exchange between cores
- Semaphore can be used to trigger modules



Note: simplified Diagram
Not all modules are shown
AXI I/F not shown

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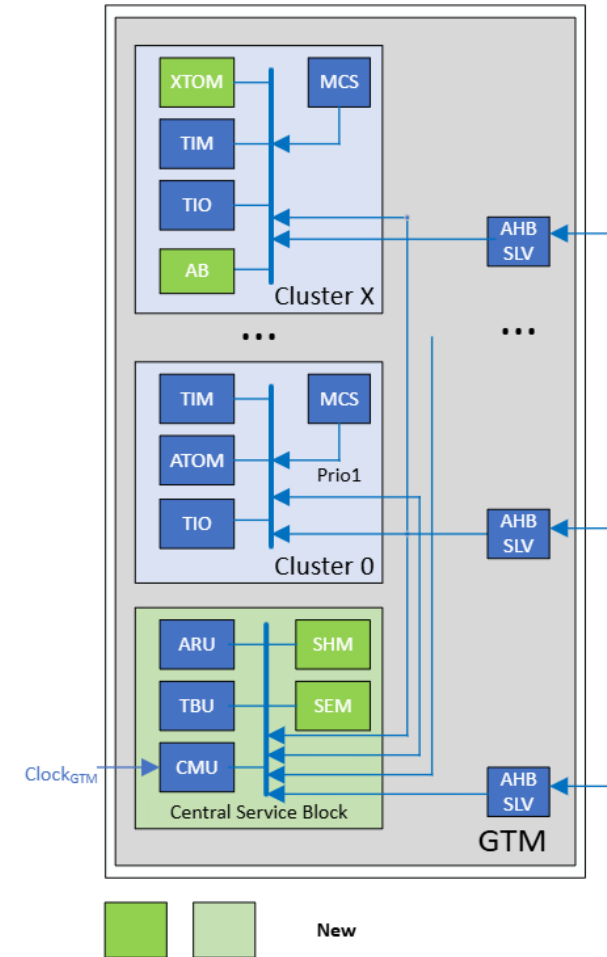
GTM Gen 5



GTM Gen 5

Phase 1 and Phase 2

- GTM standard configuration
 - A set of standard configuration will be available
- GTM custom configuration
 - Customer can use excel sheet to configure custom config
- Integration Testbench

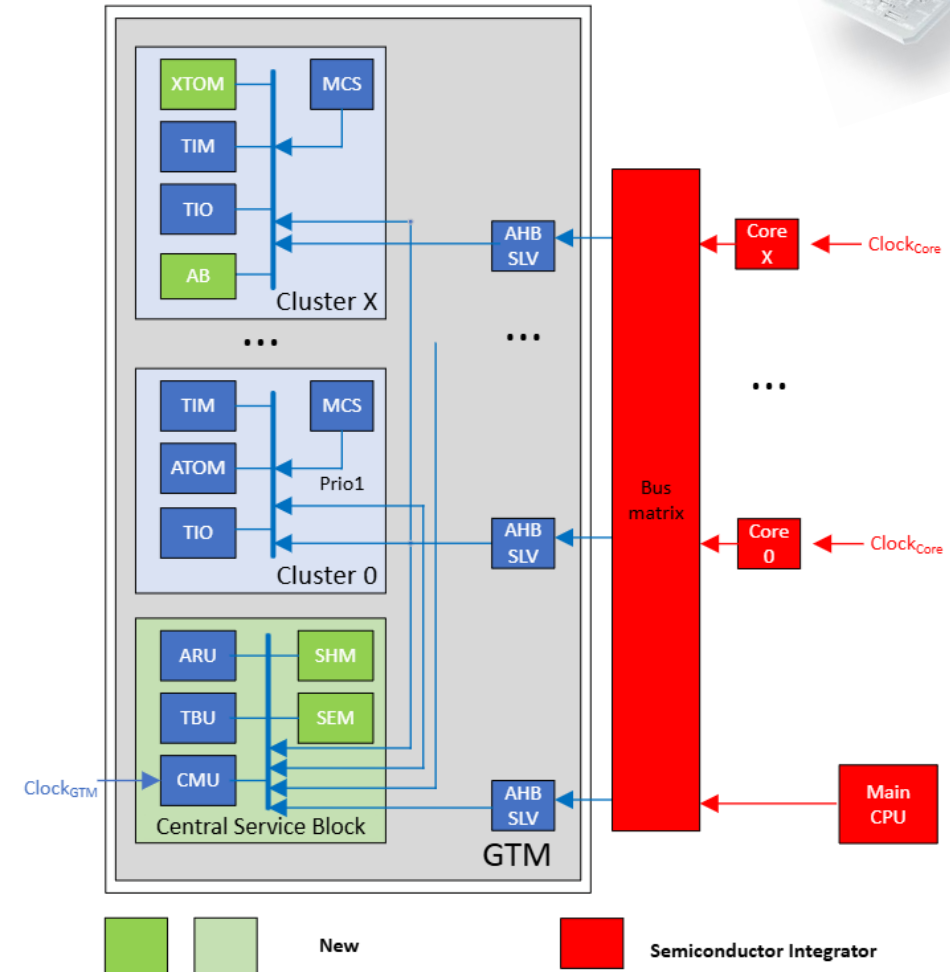


Optimization of the GTM Structure

External Core / CPU / Bus matrix

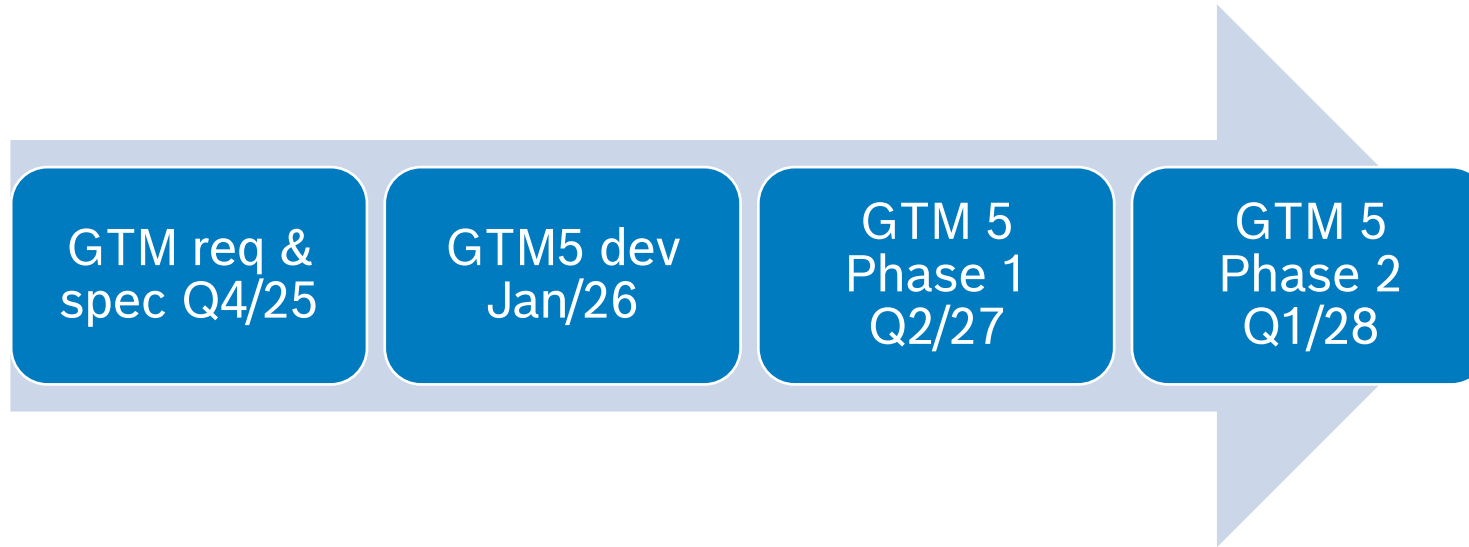
GTM implementations options by semiconductor integrator

- Bus matrix / NoC of choice
- Interface of their choice
- Cores of their choice



GTM Roadmap

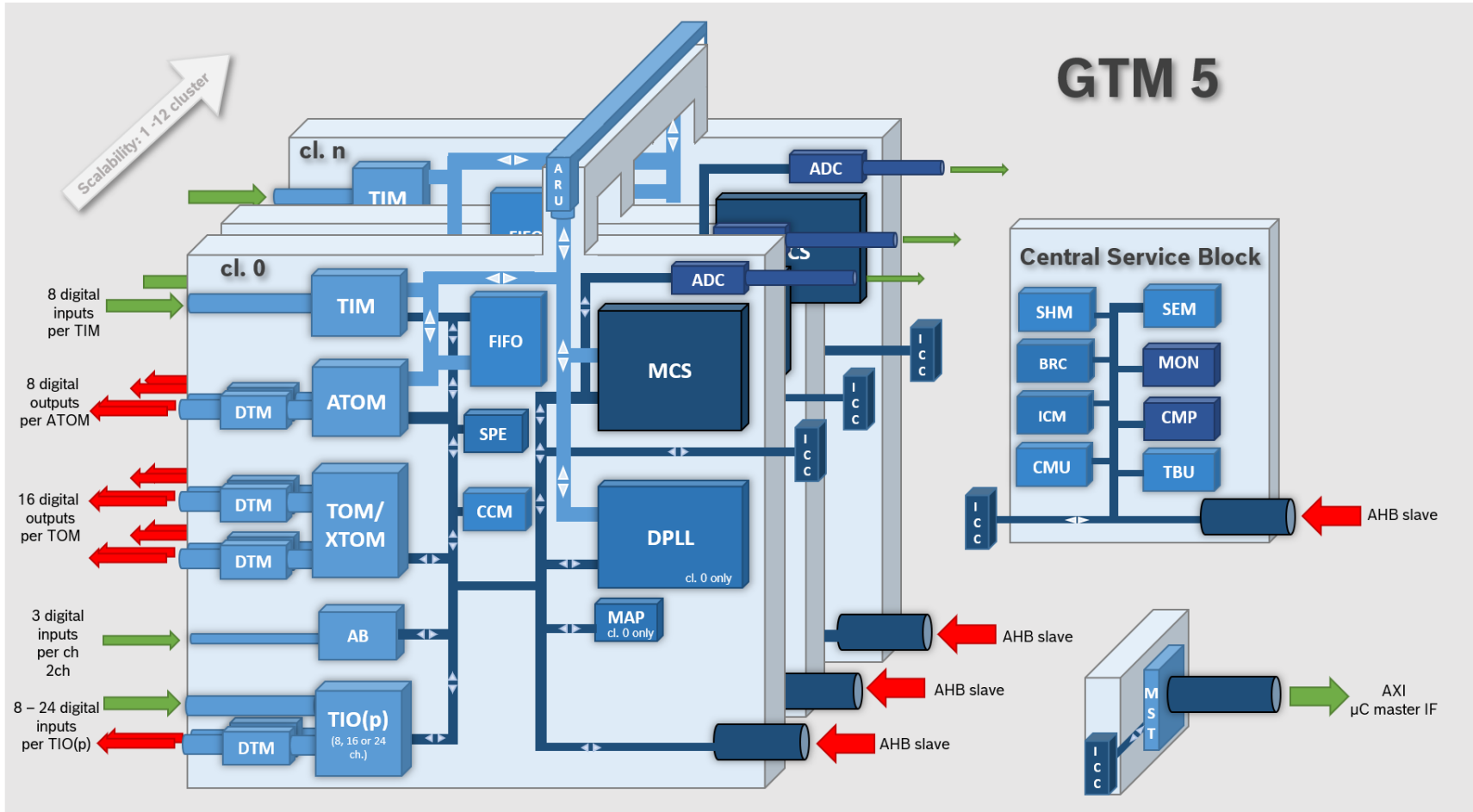
GTM 5 Timeline



Preliminary timeline: Timeline can change without notification
GTM is in /development, Features can change without notification
Intermediate deliveries will be made available.

GTM Gen 5

Overview



- ◀▶ AHB bus – intra cluster & μ C communication
- ◀▶ ARU bus – intra & inter cluster communication

- I/O modules:**
- Timer Input Module (8 ch.)
 - Timer Output Module (16 ch.)
 - eXtended Timer Output Module (16 ch.)
 - Timer Input/Output Module (8 – 24 ch.)
 - ARU connected Timer Output Module (8 ch.)
 - Dead Time Module
 - AB decoder
- Core module:**
- Multi Channel Sequencer (8 ch.)
- Special Function modules:**
- Digital Phase Locked Loop (DPLL)
 - Sensor Pattern Evaluation (SPE)
 - MAPping module
 - Analog/Digital Converter I/F
 - Share Memory Module (SHM)
 - Semaphore (SEM)
- Infrastructure modules**
- Clock Management Unit (CMU)
 - Cluster Configuration Module (CCM)
 - Time Base Unit (TBU)
 - Broadcast Unit (BRC)
 - Interrupt Concentrator Module (ICM)
- Safety modules:**
- output CoMPare unit (CMP)
 - MONitor unit (MON)

GTM Gen 5

GTM 5.0 | Key takeaways

Established base

Automotive quasi-standard – broad MCU adoption and application coverage
Scalable architecture – 1–12 clusters from low- to high-end

Gen 5 drivers

Electrification, performance and isolation – the priorities shaping the new architecture

Phase 1

Central Service Block + AHB I/F per-cluster – faster, parallel register access
Freedom of Interference – stronger partitioning
AB Decoder – Motor control w/ AB decoding

Phase 2

XTOM – advanced PWM and synchronized multi-channel updates
SHM + SME – shared data and safe inter-core coordination

Compatibility

Legacy modules stay unchanged – applications from GTM Gen 1–4.1 remain supported

Delivery

Standard and custom configurations; Phase 1 release planned for Q2/2027



THANK YOU!