XCAN IP-MODULE OVERVIEW

BOSCH

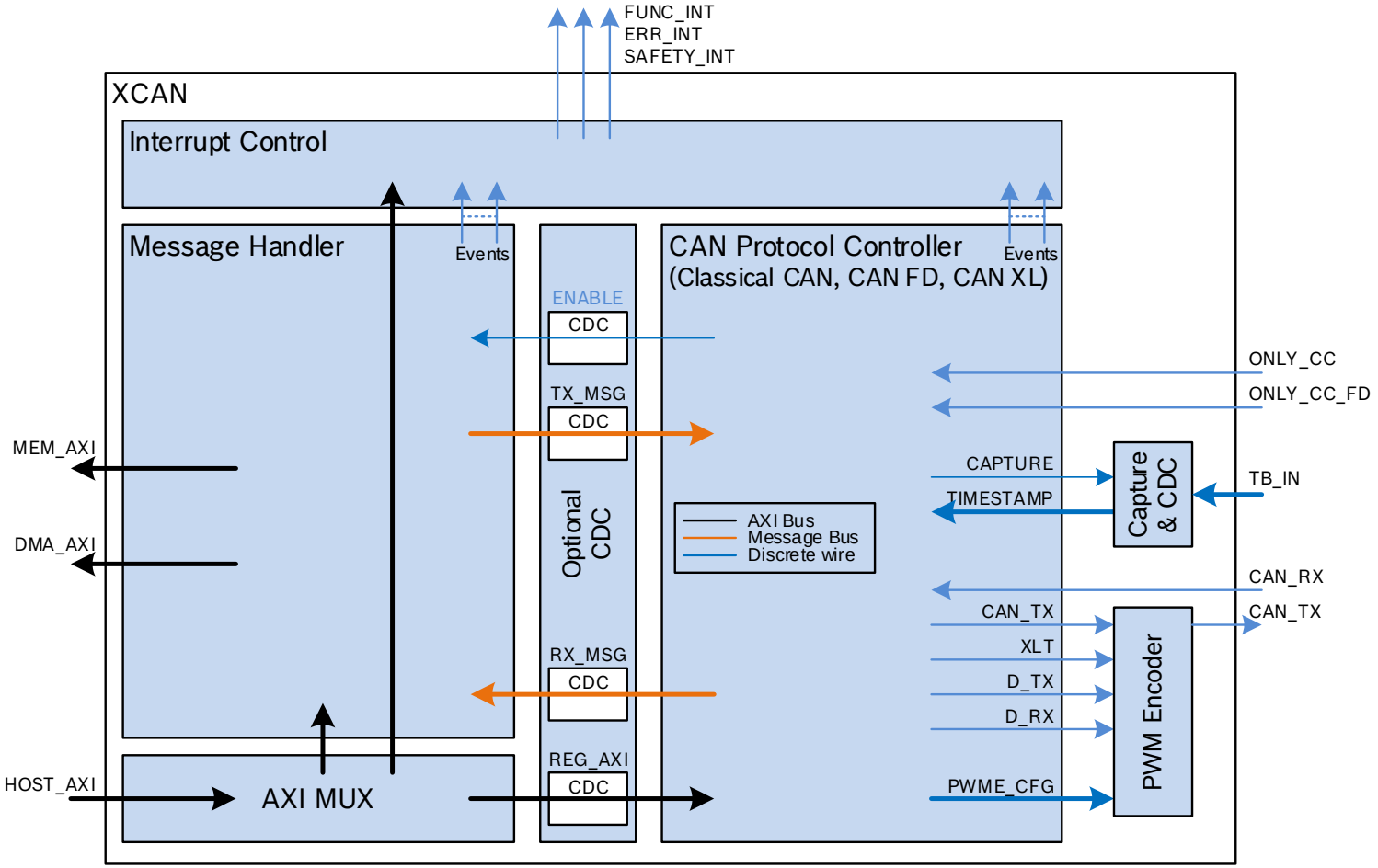
XCAN Overview

FEATURES

- Support of Classical CAN, CAN FD, and CAN XL
- Full support of CAN XL protocol with payloads up to 2048 bytes
- Small local memory (4 kbytes considering 256 filter elements and 256 references defined)
- Message storage in system memory
- Internal DMA engine, XCAN acts as DMA master for message handling
- AXI4 DMA system, bus interface 32bit, max. burst size of 8x32bit
- Low CPU impact, any accesses to/from the system memory are done using the internal DMA engine (less interrupts)
- 8 RX FIFO queues (FIFO queue defined using link list)
- RX filtering with up to 256 advanced filter elements (2 matches per filter element with up to 256 references value/mask)
- 8 TX FIFO queues (FIFO queue defined using link list)
- 1 TX priority queue, up to 32 slots, configurable by SW
- TX filtering capabilities to support security
- 64-bit Timestamps from external Timebase
- Privileged accesses to protect configuration and RX/TX filtering (optional)

Minor adjustments possible!

XCAN Overview
Block diagram



XCAN Overview
XCAN Interface

Signal	Dir	Function
HOST_AXI	I/O	RD/WR access to config/control/status registers
DMA_AXI	I/O	DMA Interface for message transfer between XCAN and System RAM
MEM_AXI	I/O	Interface to local Message RAM
FUNC_INT	O	Functional Interrupt
ERR_INT	O	Error Interrupt
SAFETY_INT	O	Safety Interrupt
CAN_RX	I	CAN receive input from transceiver
CAN_TX	O	CAN transmit output to transceiver
TB_IN	I	Time Base Input from external counter for 64-bit time stamping
ONLY_CC_FD	I	If fixed to '1' only Classical CAN and CAN FD operation enabled
ONLY_CC	I	If fixed to '1' only Classical CAN operation enabled

XCAN Overview
XCAN is DMA Master

- Advantages
  - Limits required local RAM size to 4 kbyte
    - Local RAM buffers part of RX/TX messages during transfer from/to system memory
    - Local RAM holds acceptance filter elements
    - Local RAM holds active descriptors for DMA transfer to system memory
  - RX/TX data stored in system memory
    - All data handled in system memory
    - No extra transfers from/to local RAM to be initiated by CPU
    - Reduced interrupt load

XCAN Overview
Timeline

- Revision 1.0.0 E/2021
  - CAN XL implemented according to final version of CiA610-1
  - Conformance Tested for Classical CAN and CAN FD

- Revision 1.0.0XL depending on availability of CAN XL CT
  - Conformance Tested for Classical CAN, CAN FD, and CAN XL

- Licensing conditions available at Bosch AE

  Please contact: Bosch.Semiconductors@de.bosch.com

THANK YOU