XS_CAN IP module

ME-IC/PRM-IP, October 2025

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IP business @ Bosch Mobility Electronics
IP Portfolio

I/O Processing IP | **Communication IPs** | **Accelerator IP**

GTM IP Gen 4

... realtime oriented I/O co-processor *(aka "Timer")*

- A scalable timer solution for ...
  - digital input data processing (e.g. sensor data)
  - digital output data generation (e.g PWMs for actor control)
- Integrated multi-threaded RISC cores for real-time oriented control loops
- Generic architecture to address multiple domains
  - Powertrain (combustion & electric)
  - Chassis and Body applications
  - Inverter, PFC,
  - ...

CAN IPs

... Controller Area Network IPs

- **X_CAN IP**
  - Triple-protocol support: *1
    - Classical CAN, CAN FD and **CAN XL (new)** and CAN FD light commander
  - Active DMA support
  - Bitrates up to 20 Mbit/s
  - Payload up to 2048 byte
- **M_CAN IP**
  - Dual-protocol support: *1
    - Classical CAN and CAN FD and CAN FD light commander
  - Bitrate up to 8 Mbit/s
  - Payload up to 64 bytes
- **XS_CAN IP**
  - Small gate count
  - Triple-protocol support:
    - Classical CAN, CAN FD and **CAN XL (new)**
  - Bitrates up to 20 Mbit/s
  - Payload up to 2048 byte
  - CAN FD light Commander up to 8Mbit/s **(new)**
- **FDLR_CAN IP**
  - CAN FD light responder IP
  - For Responder Nodes, MCU less
  - Bitrate up to 8 Mbit/s
  - Payload up to 64 bytes

CAN protocol licensing

- CAN FD (light) protocol license
- CAN XL protocol license

*1, CAN FD light Commander up to 1 Mbit/s

DFA IP Data Flow Architecture

... HW based accelerator for advanced mathematical algorithms

- Ready for AI & ML (**A**rtificial **I**ntelligence, **M**achine **L**earning)
- Data-based modeling, signal processing, control theory, physical equations
- Enabler for new compute-intensive functions e.g. novel features + legal regulations like EU7, OBM

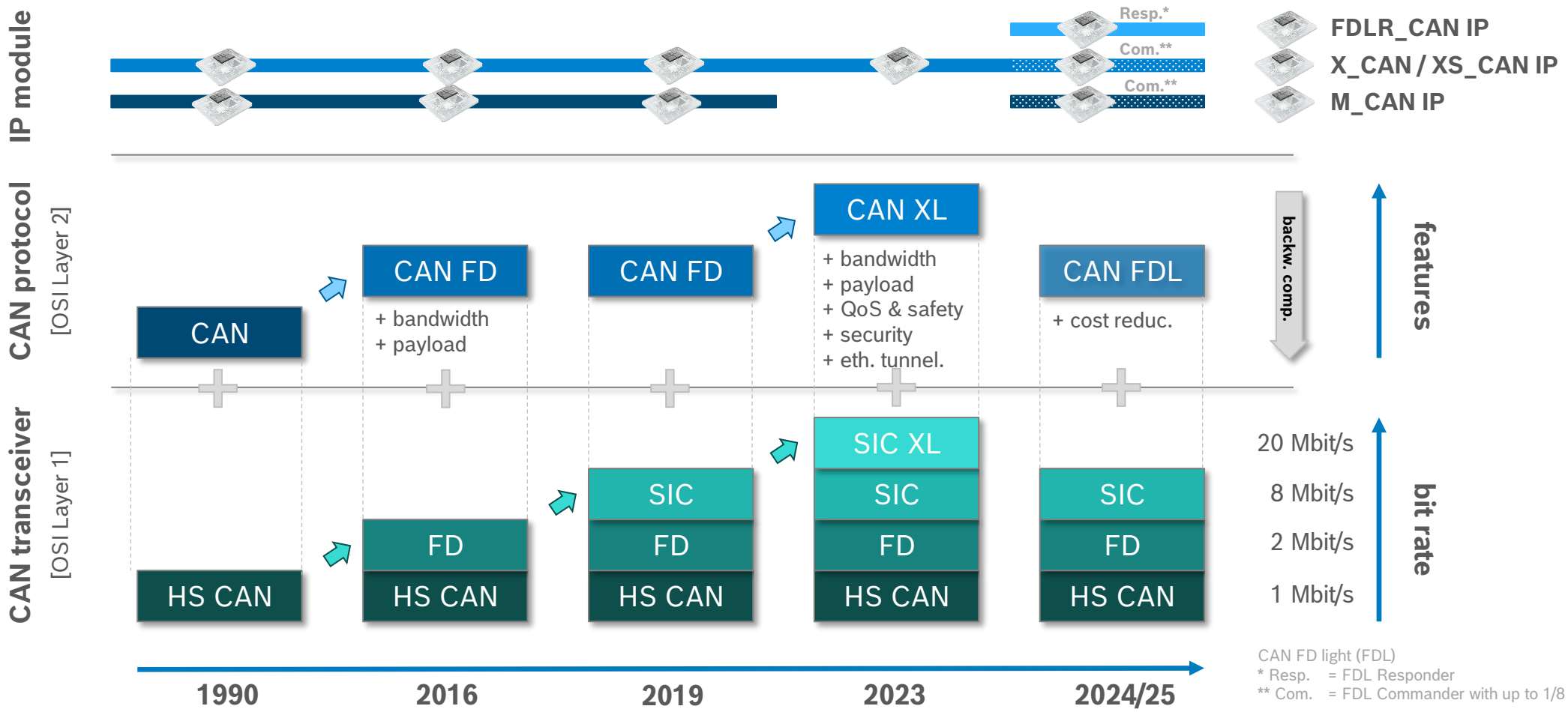
Computer Vision IP Gen 2

... comprehensive set of computer vision processing elements

- Optical Flow
  - Optical flow field estimation
  - Native 12MPix input image resolution support
  - Nearly one flow vector per pixel
  - Camera's ego-motion estimation
- Stereo Disparity module
- Classifier Engine
- Structure from Motion Detection

IP business @ Bosch ME

CAN roadmap



CAN FD light (FDL)
* Resp. = FDL Responder
** Com. = FDL Commander with up to 1/8 Mbit/s

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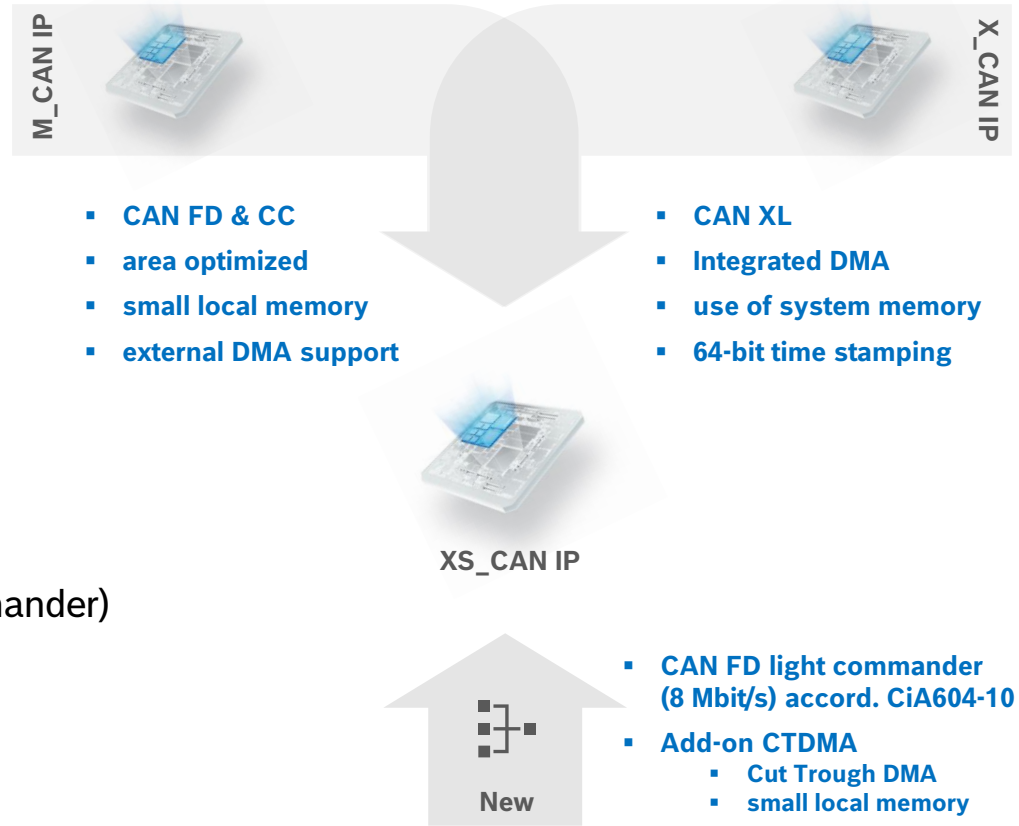
XS_CAN Overview

XS_CAN
Key Properties

XS_CAN combines key benefits of existing CAN IP modules in new area optimized solution

- Low gate count
  - Enables CAN XL use in small devices
  - Enables multi-/many- port products at low area demand
  - Only small local memory required (1-2kbyte)
- Supports system resources (DMA, system memory)
  - DMA friendly interfaces
- Supports all CAN types
  - ISO 11898-1:2024: CAN **XL, FD, CC** and **CAN FD light** (commander)
  - CiA 604-10: **CAN FD light** commander up to **8 Mbit/s**



XS_CAN Overview
XS_CAN IP – Basic Idea

XS_CAN IP Main Submodules

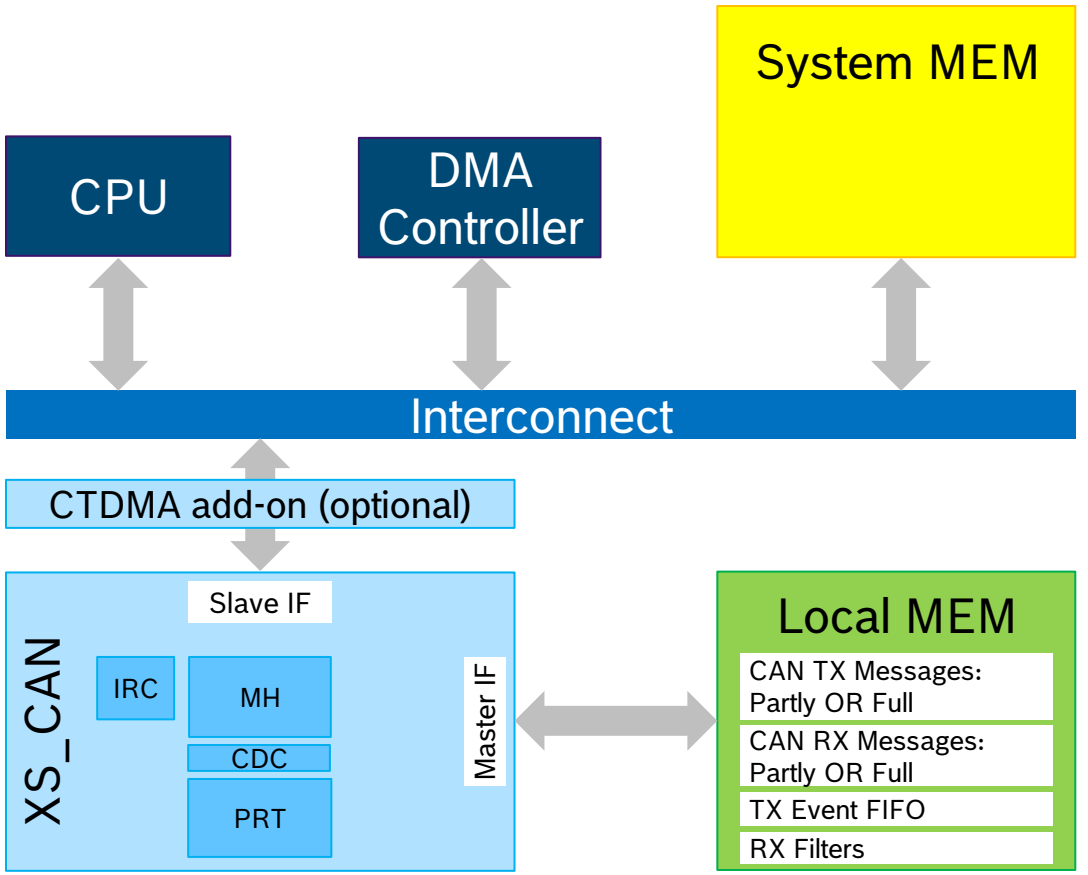
- Protocol Controller (PRT)
- Message Handler (MH)
- Clock Domain Crossing (CDC)
- Interrupt Controller (IRC)

Basic Idea

- Local Memory (LMEM) used for data storage (like M_CAN)

- Two modes of operation (software configurable)
  - **Full Message Mode (FMM)**
    - LMEM contains queues in RX/TX direction (like M_CAN)
  - **Cut-Through Mode (CTM, only usable with CTDMA)**
    - LMEM contains queues only partly
    - System Memory (SMEM) used for CAN message storage
    - Usable with all frame formats: CC, FD, XL

- CTDMA add-on (optional)
  - is a hardware accelerator to perform fast copy operation between LMEM and SMEM
  - can be shared by 4 XS_CANs



CAN IP Modules
Comparison of Features

Feature	M_CAN + DMU & TSU add-on	X_CAN	XS_CAN + CTDMA add-on
Top			
Host Interface	Slave	Slave & Master	Slave & Master (via CTDMA)
Local MEM required	yes	yes	yes (small due to CTDMA)
Virtual buffers (DMA friendly)	yes	not required	yes
Safety Features	no	yes (ASIL D capable*1)	yes (ASIL D capable*1)
Time Stamping	32 bit	64 bit	64 bit
Message Handling			
TX Priority Queue	1	1	1
TX FIFO Queue	1	8	1
TX Event FIFO Queue	1	not required	1
RX FIFO	2	8	2
RX Filters	64 + 128	255	127 double
Protocol Controller			
CAN Protocols	CC, FD, FD light*2	CC, FD, FD light*2, **XL**	CC, FD, **XL**, **FD light 8 Mbit/s**

The XS_CAN is optimized on gate count.

It combines best features of M_CAN and X_CAN.

*1 with external measures
*2 up to 1 Mbit/s

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CAN XL in resource limited end nodes
Optimization step 1: Storage Location realized with XS_CAN

Full Message Mode (FMM)

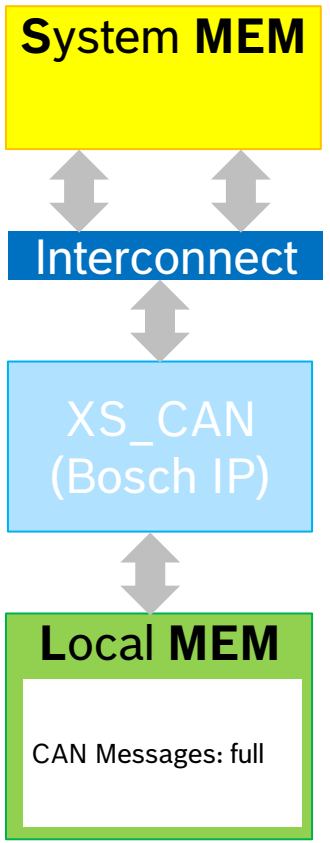
Idea

a) Keep CAN messages locally in LMEM.

b) CPU/DMA enqueues/ dequeues messages to LMEM.

Drawback

When CAN XL message size of 2048 byte is to be supported, LMEM size gets big, > 5 kbyte



Cut Through Mode (CTM)

Idea

a) CTDMA module copies messages on the fly between SMEM ⇔ LMEM

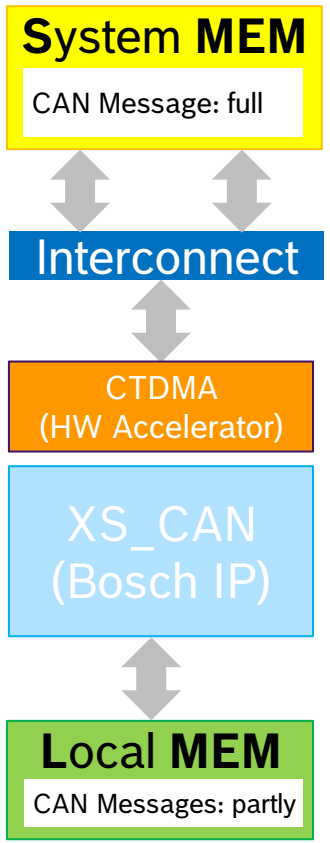
b) SMEM holds full messages, LMEM holds messages partly

c) Reduce LMEM size, increase SMEM size

Advantage

LMEM size of 2 kbyte is sufficient for nearly all use cases. 1 kbyte LMEM also possible.

Gate count for CTDMA + memory is lower than w/o CTDMA for larger messages.



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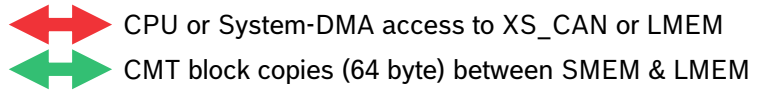
Add-on: CTDMA

XS_CAN
CTDMA **as local IP**

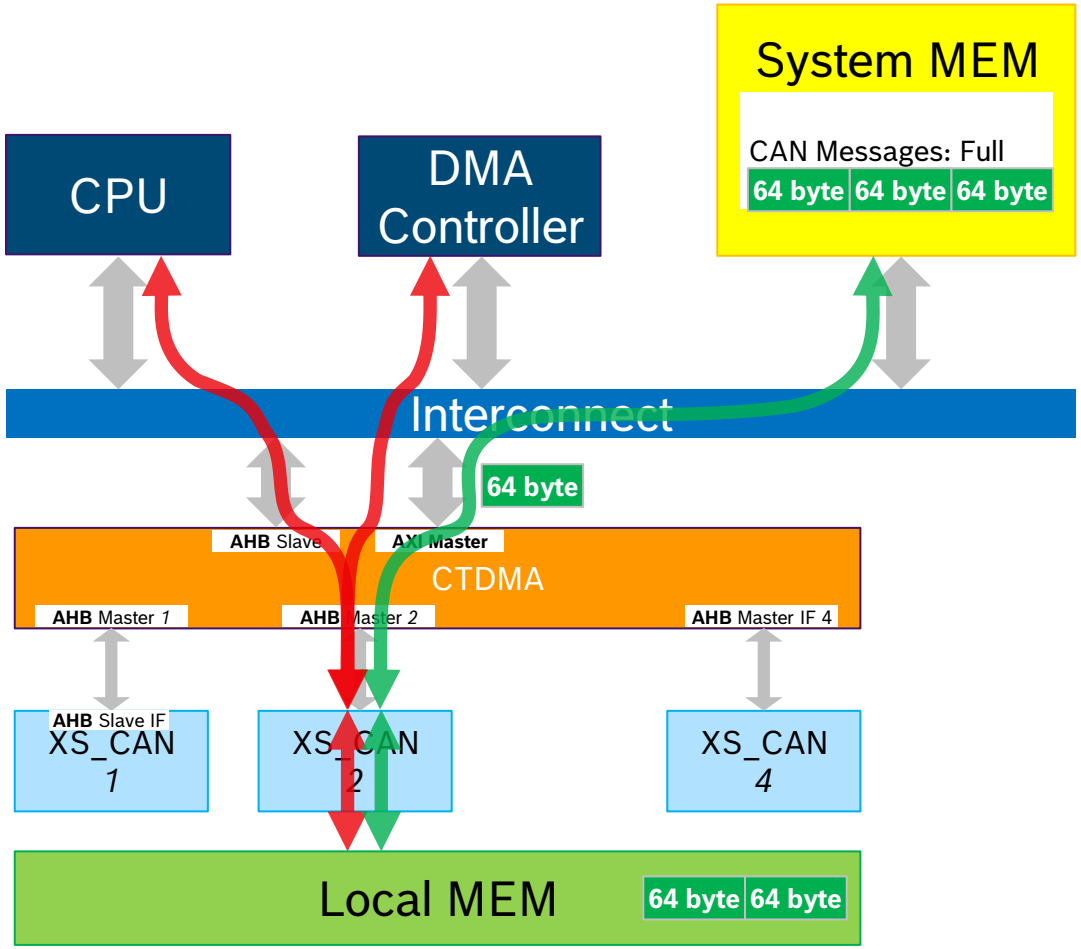


Details

- Is a hardware accelerator optimized for XS_CAN
- Can be shared by up to 4 XS_CANs
- CTDMA performs “64 byte” copies between LMEM ⇔ SMEM
- XS_CAN provides source & destination address via signals to CTDMA (relaxes time budget for copy operation)

Advantages

- Small LMEM of 1-2 Kbyte is sufficient (reduction by 80%)
- Total gate count (IP + LEMEM) significantly decreases
- Gate count (IP + LMEM) decreases below “CAN FD level” used in M_CAN despite the large CAN XL frames
- CTDMA supports CC, FD, XL messages (same handling of all)



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XS_CAN IP

XS_CAN Overview

FEATURES

- Support CAN CC, CAN FD, CAN FD light and CAN XL
  - Conform with ISO 11898-1 and CiA 604-10
- Full support of CAN XL protocol
  - Up to 20Mbit/s and up to 2048 bytes
- Support of CAN FD light Commander
  - Up to 8 Mbit/s (based on CiA604-10)
- FMM - Full Message Mode
  - Complete messages stored in the local memory (LMEM)
- CTM – Cut Trough Mode
  - RX messages are streamed to SMEM (no storage in LMEM)
  - TX messages are partly stored in LMEM (first 64 bytes), rest is streamed from SMEM in 64-byte blocks
  - Only Small local memory needed
  - Only usable with CTDMA add-on
- CTDMA (Cut-Trough DMA) Add-on module
  - DMA optimized for XS_CAN in CTM mode

- 2x RX FIFO queues, with up to 255 messages
- 1x TX FIFO queue, with up to 255 messages
- 1x TX Priority queue, up to 32 slots
- 1x TX Event FIFO queue with up to 64 events
- 127 RX Filters w/ 254 reference value-mask on first 8 byte of a message
- 64-bit Timestamps from external Timebase
- Local Memory Size
  depends and use case and queue lengths
  - Small: FMM with CC and FD
  - Medium: FMM with CC, FD, XL with short Queues
  - Small: CTM with CC, FD, XL with long Queues

XS_CAN Overview

FEATURES

- Host interface (slave): AHB 32-bit, AMBA 2 ARM Ltd protocol
- LMEM interface (master): SRAM I/F

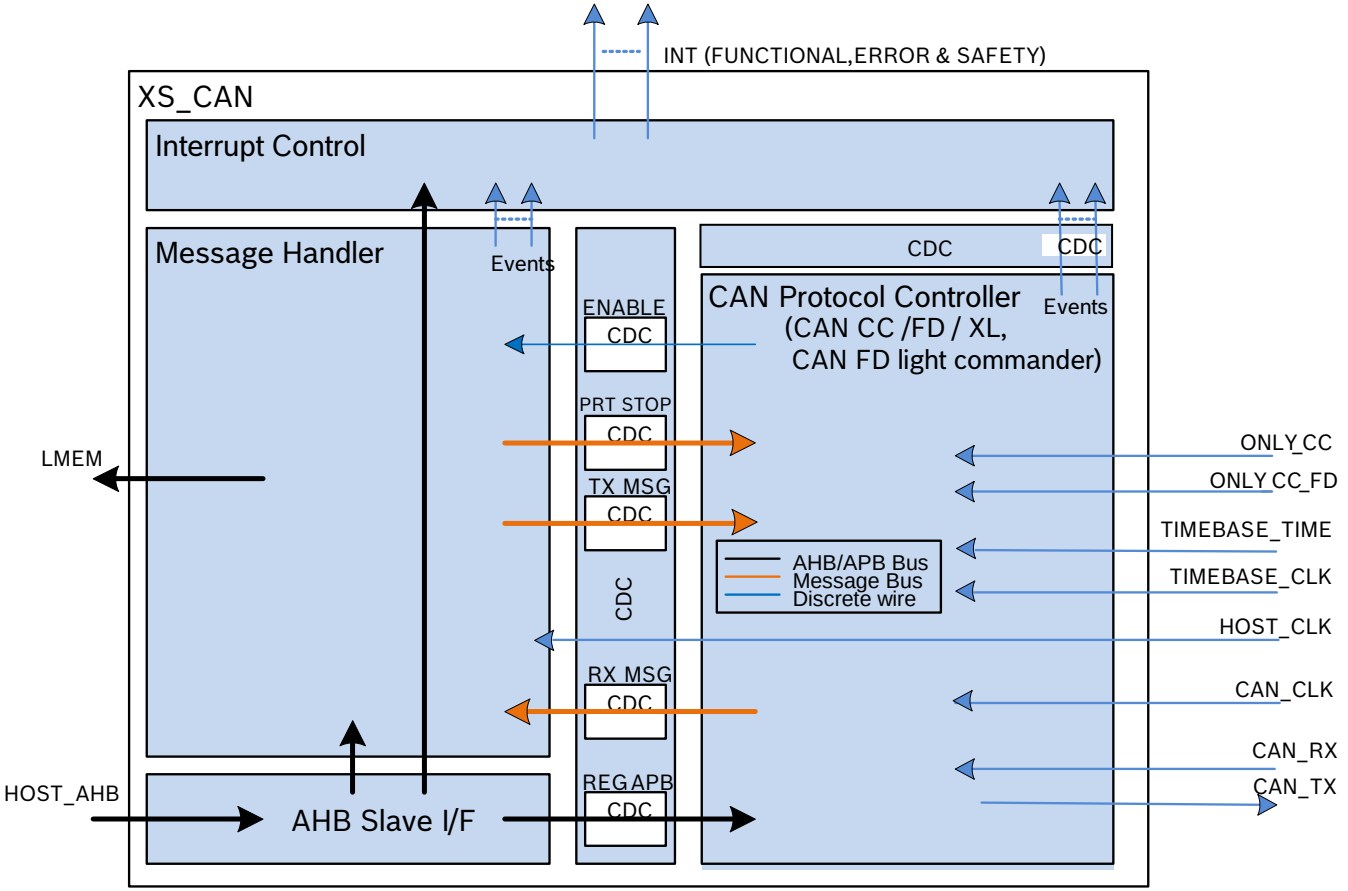
- Multiple XS_CAN can share the same Local Memory
- Maskable module interrupts with four categories:
  Rx Functional, Tx Functional, Error/Status, and Safety
- Three clock domains: HOST, CAN, Timebase
- Power-down support

- ASIL D capable with external measures
- ISO 21434 capable with external measures

- CAN Error Logging
- Fault Injection Module
  enable to transmit erroneous frames for test purposes
- Programmable loop-back test mode

- Prepared for use of Transceiver Sharing:
  allows one physical transceiver interface in MCU to be shared between several XS_CANs

XS_CAN Overview
Block diagram (simplified)



Signal	Dir	Function
HOST_AHB	I/O	RD/WR access to config/control/status registers and LMEM
LMEM	I/O	Interface to local Message RAM
INT	O	Interrupt (Functional, Error, Safety)
ONLY_CC	I	If fixed to '1' only Classical CAN operation enabled
ONLY_CC_FD	I	If fixed to '1' only Classical CAN and CAN FD operation enabled
TIMEBASE_TIME	I	Time value of external time base
TIMEBASE_CLK	I	Timebase clock
HOST_CLK	I	Host clock (MH, INT, LMEM I/F, AHB I/F)
CAN CLK	I	CAN clock for the PRT
CAN_RX	I	CAN receive input from transceiver
CAN_TX	O	CAN transmit output to transceiver

Glossary:
- CDC - Clock Domain Crossing

XS_CAN Overview
Timeline & Deliverables

Revision 1.0.0
Available 07/25
Only FMM mode

Revision 1.1.0
Planned Q1/26
FMM and CTM mode

Deliverables include:

- VHDL Source Code
- User Manual (programmer's view)
- Module Integration Guide (designer's view)
- FMEDA
- Safety Manual*1
- Security Manual*1
- Functional Safety assessment certificate
- Conformance Test Report for CAN and CAN FD *2
- Conformance Test Report for CAN XL*2

Licensing conditions available at Bosch AE
Please see: https://www.bosch-semiconductors.com/ip-modules/can-protocol-license/

Add-on CTDMA
Planned Q1/26

Deliverables include:

- VHDL Source Code
- User Manual (programmer's view)
- Module Integration Guide (designer's view)
- FMEDA
- Safety Manual
- Security Manual
- Functional Safety assessment certificate

*1 Safety and Security Manual will be provided in Q1/26 with the release of the CTDMA

*2 Conformance test when available by test house, planned Q1/26

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Introduction of
- CAN XL
- CAN FD light

CAN XL – Next Step in CAN Evolution

Superior up to 20 Mbit/s network solution

IP available

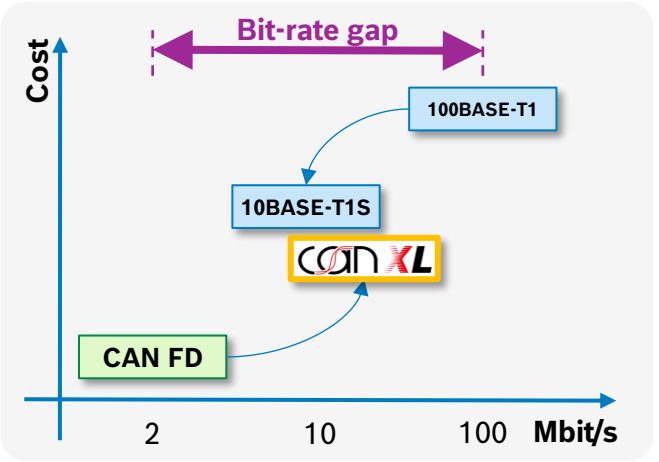
Broad availability in nextGen µCs

Target / Motivation

Provide a superior ≤20Mbit/s CAN solution with respect to

- Price (Transceiver, Pins, Cabling, ...)
- Safety and Security
- Enables SOA (Service Oriented Architecture)
- Quality of Service

Preserve CAN properties: Arbitration, robustness, long stubs, ...



Compatibility of CAN FD and XL enables ...

- Incremental upgrade path

  ➔ larger acceptance - re-use of CAN / CAN FD knowhow and equipment
- E/E Architecture design freedom: "mixed FD/XL" or "XL only" networks:
  - "XL only" networks up to 20 Mbit/s
  - "mixed" networks limited to 8 Mbit/s (e.g. XL 8 Mbit/s, FD 2 Mbit/s)

Key Success Factors

1) **Cost Optimal E/E Architectures**
   Single bus for 3 types of traffic
   (CAN FD, CAN XL and Ethernet)
2) **Bit rate up to 20 Mbit/s**
   Compatible with wide range of transc.
   (HS-CAN, FD, SIC, SIC XL)
3) **Large payload size (1 .. 2048 bytes)**
   enough space for any application
4) **Ethernet Tunneling**
   allows use of TCP/IP, SOME/IP, etc.
5) **Incremental upgrade**
   Allows CAN FD and CAN XL on the same network (up to 8 Mbit/s)
6) **Scalable**
   flexible tradeoff between cost, speed and network complexity
7) **Broad availability**
   majority of nextGen automotive µCs

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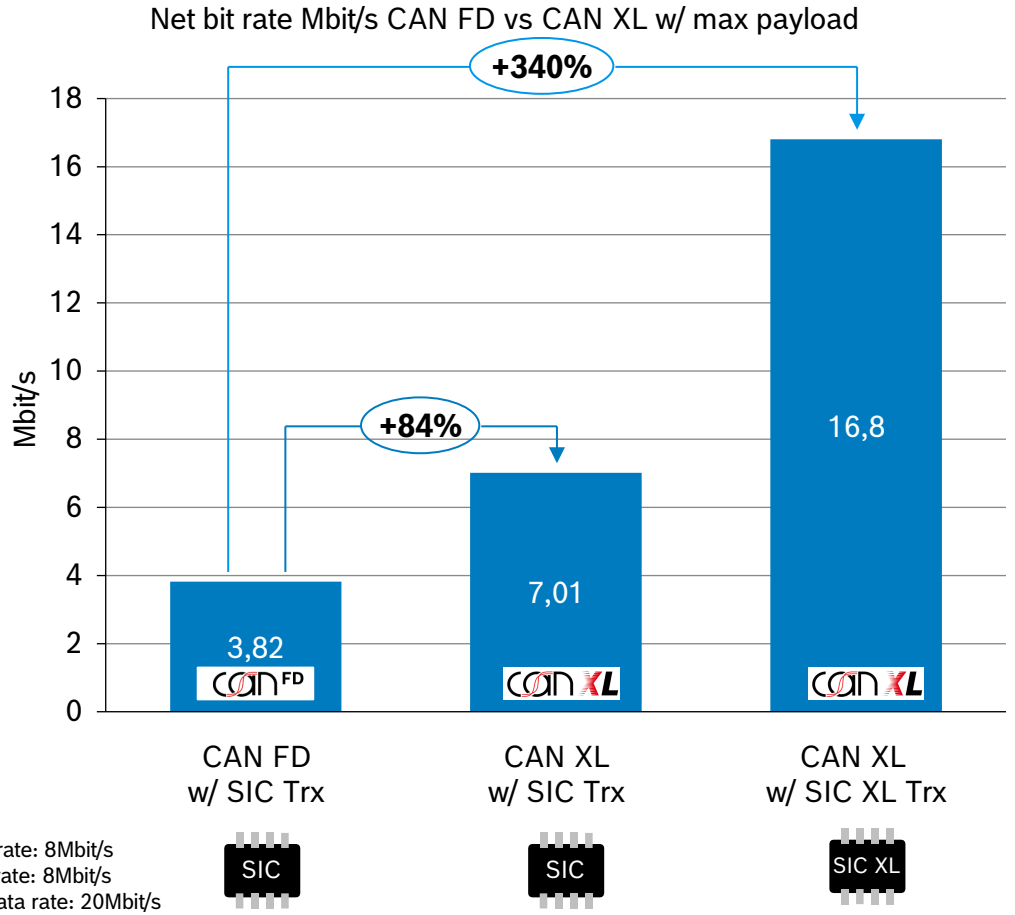
CAN XL – Next Step in CAN Evolution
CAN XL more efficient than CAN FD

84% performance increase

- CAN XL compared to CAN FD at the **same cost** w/ CAN SIC Trx at 8 Mbit/s
  - Same: cable, transceiver, external components
  - Cost is determined by the external component cost!
  - CAN XL is more efficient as data payload is 2048 byte

340% performance increase

- with CAN XL w/ CAN SIC XK Trx (20 Mbit/s) compared to CAN FD w/ CAN SIC Trx (8 Mbit/s)
  - Minimal Cost adder CAN SIC -> CAN SIC XL

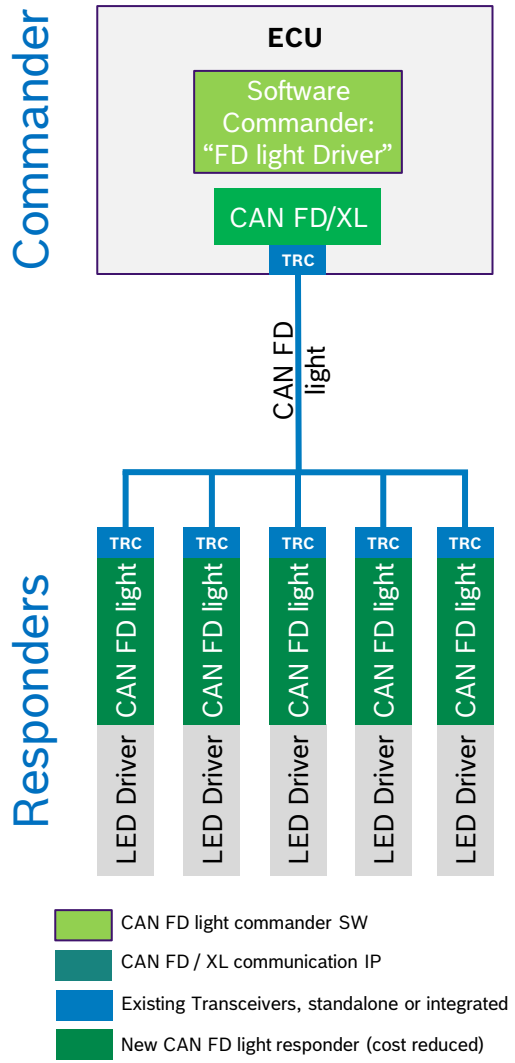


CAN FD w/SIC Trx: ID: 11bit, Arbitration: 500 Kbit/s, Data rate: 8Mbit/s
CAN XL w/SIC Trx: ID: 11bit, Arbitration: 500 Kbit/s, Data rate: 8Mbit/s
CAN XL w/SIC XL Trx: ID: 11bit, Arbitration: 500 Kbit/s, Data rate: 20Mbit/s

CAN FD light
What is CAN FD light?

CAN FD light is a cost optimized CAN FD (≈50% reduction)

- **Architecture:** *1*x Commander and *N*x Responders
  - CAN FD light commander controls communication (polling)
- **Commander:** All existing CAN FD/XL nodes (M_CAN /X_CAN/XS_CAN)
- **Responder:** low-cost CAN FD node
  - [Layer 1] No change, all CAN transceivers usable
  - [Layer 2] Simplified Protocol: sub-set of CAN FD
    - **No** arbitration, **No** error frames, **No** 29 Bit ID, **No** BRS bit rate switch…
    - **CAN FD frame format** with 11 Bit ID **used**
    - Standardized in ISO 11898-1:2024
- **Advantages**
  - Low-Cost (e.g. clock with ±4% usable, x10 more than FD ➔ Save 0,40 US$)
  - Monolithic integration possible of (1) Transceiver, (2) CAN FD light IP, (2) analog part
  - Larger net bit rate of CAN FD light then CAN FD



THANK YOU!

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